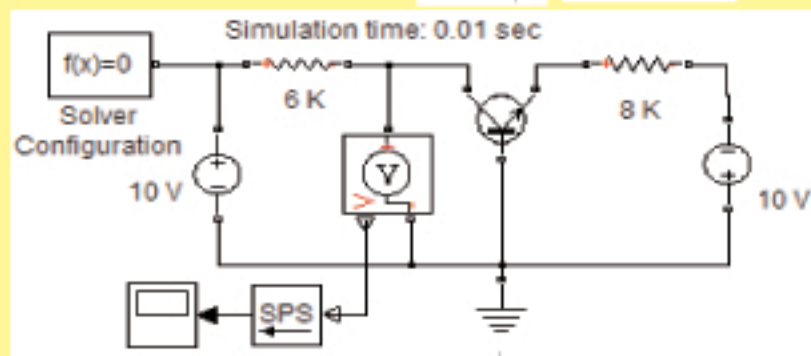


Electronic Devices and Amplifier Circuits

Third Edition

Steven T. Karris



MATLAB®
and Simulink®
examples

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Electronic Devices and Amplifier Circuits

with MATLAB®/Simulink® Examples

Third Edition

Students and working professionals will find *Electronic Devices and Amplifier Circuits with MATLAB® / Simulink® Examples*, Third Edition, to be a concise and easy-to-learn text. It provides complete, clear, and detailed explanations of the state-of-the-art electronic devices and integrated circuits. All topics are illustrated with many real-world examples.

This text includes the following chapters and appendices:

- Basic Electronic Concepts and Signals • Introduction to Semiconductor Electronics - Diodes
- Bipolar Junction Transistors • Field Effect Transistors and PNP Devices • Operational Amplifiers
- Integrated Circuits • Pulse Circuits and Waveforms Generators • Frequency Characteristics of Single-Stage and Cascaded Amplifiers • Tuned Amplifiers • Sinusoidal Oscillators • Introduction to MATLAB® • Compensated Attenuators • The Substitution, Reduction, and Miller's Theorems

Each chapter contains numerous practical applications supplemented with detailed instructions for using MATLAB to plot the characteristics of non-linear devices and to obtain quick solutions.

Each chapter and appendix contains numerous practical applications supplemented with detailed instructions for using MATLAB and Simulink to obtain accurate and quick solutions.



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Preface

This text is an undergraduate level textbook presenting a thorough discussion of state-of-the-art electronic devices. It is self-contained; it begins with an introduction to solid state semiconductor devices. The prerequisites for this text are first year calculus and physics, and a two-semester course in circuit analysis including the fundamental theorems and the Laplace transformation. No previous knowledge of MATLAB® is required; the material in Appendix A and the inexpensive MATLAB Student Version is all the reader needs to get going. The discussions are based on a PC with the Windows 7 platform but if you have another platform such as Macintosh, please refer to the appropriate sections of the MATLAB's User Guide which also contains instructions for installation. Additional information including purchasing may be obtained from The MathWorks, Inc., 3 Apple Hill Drive, Natick, MA 01760-2098. Phone: 508 647-7000, Fax: 508 647-7001, e-mail: info@mathwork.com and web site <http://www.mathworks.com>. Even though this text can also be used without MATLAB, it is highly recommended to be used with the inexpensive MATLAB Student Version. The MATLAB scripts in this text are available free of charge upon request. Contact us at info@orchardpublications.com.

This is our fourth electrical and computer engineering-based text with MATLAB applications. My associates, contributors, and I have a mission to produce substance and yet inexpensive texts for the average reader. Our first three texts* are very popular with students and working professionals seeking to enhance their knowledge and prepare for the professional engineering examination.

The author and contributors make no claim to originality of content or of treatment, but have taken care to present definitions, statements of physical laws, theorems, and problems.

Chapter 1 is an introduction to the nature of small signals used in electronic devices, amplifiers, definitions of decibels, bandwidth, poles and zeros, stability, transfer functions, and Bode plots. Chapter 2 is an introduction to solid state electronics beginning with simple explanations of electron and hole movement. This chapter provides a thorough discussion on the junction diode and its volt-ampere characteristics. In most cases, the non-linear characteristics are plotted with simple MATLAB scripts. The discussion concludes with diode applications, the Zener, Schottky, tunnel, and varactor diodes, and optoelectronics devices. Chapters 3 and 4 are devoted to bipolar junction transistors and FETs respectively, and many examples with detailed solutions are provided. Chapter 5 is a long chapter on op amps. Many op amp circuits are presented and their applications are well illustrated.

* These are *Circuit Analysis I with MATLAB® Computing and Simulink®/SimPowerSystems® Modeling*, ISBN 978-1-934404-17-1, *Circuit Analysis II with MATLAB® Computing and Simulink®/SimPowerSystems® Modeling*, ISBN 978-1-934404-19-5, and *Signals and Systems with MATLAB® Computing and Simulink® Modeling*, ISBN 978-1-934404-23-2.

The highlight of this text is Chapter 6 on integrated devices used in logic circuits. The internal construction and operation of the TTL, NMOS, PMOS, CMOS, ECL, and the biCMOS families of those devices are fully discussed. Moreover, the interpretation of the most important parameters listed in the manufacturers data sheets are explained in detail. Chapter 7 is an introduction to pulse circuits and waveform generators. There, the 555 Timer, the astable, monostable, and bistable multivibrators, and the Schmitt trigger are discussed

Chapter 8 discusses the frequency characteristic of single-stage and cascade amplifiers, and Chapter 9 is devoted to tuned amplifiers. Sinusoidal oscillators are introduced in Chapter 10.

This is the third edition of this title, and includes several Simulink, SimPowerSystems, and SimElectronics models. Appendix A, is an introduction to MATLAB®. Appendix B is an introduction to Simulink, Appendix C is an introduction to Simscape® toolbox that includes SimPowerSystems® and SimElectronics® libraries, Appendix D is an introduction to Proportional-Integral-Derivative (PID) controllers, Appendix E describes uncompensated and compensated networks, and Appendix F discusses the substitution, reduction, and Miller's theorems.

The author wishes to express his gratitude to the staff of The MathWorks™, the developers of MATLAB® and Simulink® for the encouragement and unlimited support they have provided me with during the production of this text.

A companion to this text, *Digital Circuit Analysis and Design with Simulink® Modeling and Introduction to CPLDs and FPGAs*, ISBN 978-1-934404-05-8 is recommended as a companion. This text is devoted strictly on Boolean logic, combinational and sequential circuits as interconnected logic gates and flip-flops, an introduction to static and dynamic memory devices. and other related topics.

Although every effort was made to correct possible typographical errors and erroneous references to figures and tables, some may have been overlooked. Our experience is that the best proofreader is the reader. Accordingly, the author will appreciate it very much if any such errors are brought to his attention so that corrections can be made for the next edition. We will be grateful to readers who direct these to our attention at info@orchardpublications.com. Thank you.

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Table of Contents

1 Basic Electronic Concepts and Signals

1.1	Signals and Signal Classifications	1-1
1.2	Amplifiers	1-3
1.3	Decibels	1-3
1.4	Bandwidth and Frequency Response.....	1-5
1.5	Bode Plots.....	1-7
1.6	Transfer Function	1-9
1.7	Poles and Zeros.....	1-10
1.8	Stability.....	1-11
1.9	Voltage Amplifier Equivalent Circuit.....	1-15
1.10	Current Amplifier Equivalent Circuit.....	1-17
1.11	Summary.....	1-19
1.12	Exercises	1-22
1.13	Solutions to End-of-Chapter Exercises	1-24

MATLAB Scripts

Pages 1-7, 1-13, 1-14, 1-16, 1-25, 1-26, 1-27, 1-29, 1-30

Simulink/SimPowerSystems/SimElectronics Models

Pages 1-32, 1-33

2 Introduction to Semiconductor Electronics – Diodes

2.1	Electrons and Holes	2-1
2.2	Junction Diode.....	2-4
2.3	Graphical Analysis of Circuits with Non-Linear Devices	2-8
2.4	Piecewise Linear Approximations	2-12
2.5	Low Frequency AC Circuits with Junction Diodes.....	2-15
2.6	Junction Diode Applications in AC Circuits	2-18
2.7	Peak Rectifier Circuits	2-30
2.8	Clipper Circuits.....	2-31
2.9	DC Restorer Circuits	2-34
2.10	Voltage Doubler Circuits	2-35
2.11	Diode Applications in Amplitude Modulation (AM) Detection Circuits	2-35
2.12	Diode Applications in Frequency Modulation (FM) Detection Circuits.....	2-36
2.13	Zener Diodes	2-37
2.14	Schottky Diode.....	2-43
2.15	Tunnel Diode.....	2-44
2.16	Varactor.....	2-46
2.17	Optoelectronic Devices	2-46
2.18	Summary.....	2-50

2.19 Exercises	2-54
2.20 Solutions to End-of-Chapter Exercises	2-59

MATLAB Scripts

Pages 2-6, 2-27, 2-28, 2-59, 2-67

Simulink/SimPowerSystems/SimElectronics Models

Pages 2-14, 2-18, 2-23, 2-24, 2-29, 2-43, 2-61

3	Bipolar Junction Transistors	
3.1	Introduction	3-1
3.2	NPN Transistor Operation.....	3-3
3.3	Bipolar Junction Transistor as an Amplifier	3-3
3.3.1	Equivalent Circuit Models – NPN Transistors.....	3-6
3.3.2	Equivalent Circuit Models – PNP Transistors.....	3-7
3.3.3	Effect of Temperature on the $i_C - v_{BE}$ – Characteristics.....	3-9
3.3.4	Collector Output Resistance – Early Voltage	3-10
3.4	Transistor Amplifier Circuit Biasing.....	3-18
3.5	Fixed Bias.....	3-20
3.6	Self-Bias	3-25
3.7	Amplifier Classes and Operation.....	3-27
3.7.1	Class A Amplifier Operation	3-30
3.7.2	Class B Amplifier Operation.....	3-33
3.7.3	Class AB Amplifier Operation.....	3-35
3.7.4	Class C Amplifier Operation	3-37
3.8	Graphical Analysis.....	3-38
3.9	Power Relations in the Basic Transistor Amplifier	3-42
3.10	Piecewise-Linear Analysis of the Transistor Amplifier.....	3-43
3.11	Incremental Linear Models	3-48
3.12	Transconductance	3-53
3.13	High-Frequency Models for Transistors.....	3-54
3.14	The Darlington Connection	3-58
3.15	Transistor Networks.....	3-59
3.15.1	h -Equivalent Circuit for the Common-Base Transistor.....	3-59
3.15.2	T -Equivalent Circuit for the Common-Base Transistor.....	3-63
3.15.3	h -Equivalent Circuit for the Common-Emitter Transistor	3-64
3.15.4	T -Equivalent Circuit for the Common-Emitter Transistor.....	3-68
3.15.5	h -Equivalent Circuit for the Common-Collector Transistor	3-69
3.15.6	T -Equivalent Circuit for the Common-Collector Transistor.....	3-75
3.16	Transistor Cutoff and Saturation Regions	3-76
3.16.1	Cutoff Region	3-76
3.16.2	Active Region	3-76
3.16.3	Saturation Region	3-77

3.17	The Ebers–Moll Transistor Model.....	3–79
3.18	Schottky Diode Clamp.....	3–83
3.19	Transistor Specifications	3–83
3.20	Summary.....	3–85
3.21	Exercises	3–89
3.22	Solutions to End-of-Chapter Exercises	3–95

MATLAB Scripts

Pages 3–12, 3–38, 3–111

Simulink/SimPowerSystems/SimElectronics Model

Page 3–99

4 Field Effect Transistors and PNP Devices

4.1	Junction Field Effect Transistor (JFET).....	4–1
4.2	Metal Oxide Semiconductor Field Effect Transistor (MOSFET).....	4–6
4.2.1	N–Channel MOSFET in the Enhancement Mode.....	4–7
4.2.2	N–Channel MOSFET in the Depletion Mode	4–12
4.2.3	P–Channel MOSFET in the Enhancement Mode	4–15
4.2.4	P–Channel MOSFET in the Depletion Mode	4–18
4.2.5	Voltage Gain	4–18
4.3	Complementary MOS (CMOS).....	4–20
4.3.1	CMOS Common–Source Amplifier.....	4–20
4.3.2	CMOS Common–Gate Amplifier.....	4–21
4.3.3	CMOS Common–Drain (Source Follower) Amplifier.....	4–21
4.4	Metal Semiconductor FET (MESFET).....	4–22
4.5	Unijunction Transistor	4–23
4.6	Diac.....	4–24
4.7	Silicon Controlled Rectifier (SCR).....	4–24
4.7.1	SCR as an Electronic Switch	4–27
4.7.2	SCR in the Generation of Sawtooth Waveforms	4–28
4.8	Triac	4–39
4.9	Shockley Diode.....	4–40
4.10	Other PNP Devices.....	4–41
4.11	The Future of Transistors.....	4–42
4.12	Summary	4–44
4.13	Exercises	4–47
4.14	Solutions to End-of-Chapter Exercises	4–49

MATLAB Scripts

Pages 4–5, 4–9

Simulink/SimPowerSystems/SimElectronics Models

Pages 4–11, 4–17, 4–37, 4–38

5 Operational Amplifiers

5.1	Operational Amplifier	5-1
5.2	An Overview of the Op Amp	5-1
5.3	Op Amp in the Inverting Mode	5-2
5.4	Op Amp in the Non-Inverting Mode	5-5
5.5	Active Filters.....	5-8
5.6	Analysis of Op Amp Circuits.....	5-11
5.7	Input and Output Resistances	5-21
5.8	Op Amp Open Loop Gain	5-24
5.9	Op Amp Closed Loop Gain	5-26
5.10	Transresistance Amplifier	5-28
5.11	Closed Loop Transfer Function	5-29
5.12	Op Amp Integrator	5-30
5.13	Op Amp Differentiator	5-34
5.14	Summing and Averaging Op Amp Circuits.....	5-37
5.15	Differential Input Op Amp	5-38
5.16	Instrumentation Amplifiers.....	5-41
5.17	Offset Nulling.....	5-43
5.18	External Frequency Compensation.....	5-43
5.19	Slew Rate	5-44
5.20	Circuits with Op Amps and Non-Linear Devices	5-45
5.21	Comparator	5-48
5.22	Wien Bridge Oscillator.....	5-49
5.23	Digital-to-Analog Converters	5-51
5.24	Analog-to-Digital Converters	5-56
	5.24.1 Flash Analog-to-Digital Converter	5-55
	5.24.2 Successive Approximation Analog-to-Digital Converter	5-57
	5.24.3 Dual-Slope Analog-to-Digital Converter.....	5-58
5.25	Quantization, Quantization Error, Accuracy, and Resolution	5-60
5.26	Op Amps in Analog Computers	5-62
5.27	Gyrator	5-65
5.28	Summary.....	5-69
5.29	Exercises	5-73
5.30	Solutions to End-of-Chapter Exercises.....	5-80

MATLAB Scripts

Pages 5-82, 5-90

Simulink/SimPowerSystems/SimElectronics Models

Pages 5-5, 5-34, 5-68

6	Integrated Circuits	
6.1	Basic Logic Gates.....	6–1
6.2	Positive and Negative Logic	6–1
6.3	Inverter.....	6–2
6.4	AND Gate.....	6–6
6.5	OR Gate.....	6–8
6.6	NAND Gate.....	6–9
6.7	NOR Gate.....	6–13
6.8	Exclusive OR (XOR) and Exclusive NOR (XNOR) Gates.....	6–15
6.9	Fan–In, Fan–Out, TTL Unit Load, Sourcing Current, and Sinking Current	6–17
6.10	Data Sheets	6–20
6.11	Emitter Coupled Logic (ECL)	6–24
6.12	NMOS Logic Gates.....	6–28
	6.12.1 NMOS Inverter.....	6–30
	6.12.2 NMOS NAND Gate	6–31
	6.12.3 NMOS NOR Gate.....	6–32
6.13	CMOS Logic Gates	6–32
	6.13.1 CMOS Inverter	6–33
	6.13.2 CMOS NAND Gate	6–34
	6.13.3 CMOS NOR Gate.....	6–34
6.14	Buffers, Tri-State Devices, and Data Buses	6–35
6.15	Present and Future Technologies.....	6–39
6.16	Summary.....	6–43
6.17	Exercises.....	6–46
6.18	Solutions to End-of-Chapter Exercises	6–49

7	Pulse Circuits and Waveform Generators	
7.1	Astable (Free-Running) Multivibrators.....	7–1
7.2	555 Timer	7–2
7.3	Astable Multivibrator with 555 Timer	7–3
7.4	Monostable Multivibrators	7–15
7.5	Bistable Multivibrators (Flip-Flops).....	7–21
	7.5.1 Fixed-Bias Flip-Flop.....	7–21
	7.5.2 Self-Bias Flip-Flop	7–24
	7.5.3 Triggering Signals for Flip-Flops	7–29
	7.5.4 Present Technology Bistable Multivibrators	7–31
7.6	Schmitt Trigger	7–32
7.7	Summary.....	7–35
7.8	Exercises.....	7–36
7.9	Solutions to End-of-Chapter Exercises	7–39

MATLAB Scripts

Pages 7–10, 7–28, 7–40, 7–41

8

Frequency Characteristics of Single–Stage and Cascaded Amplifiers

8.1	Properties of Signal Waveforms.....	8–1
8.2	Transistor Amplifier at Low Frequencies	8–5
8.3	Transistor Amplifier at High Frequencies	8–9
8.4	Combined Low- and High–Frequency Characteristics	8–14
8.5	Frequency Characteristics of Cascaded Amplifiers	8–14
8.6	Overall Characteristics of Multistage Amplifiers.....	8–25
8.7	Amplification and Power Gain in Three or More Cascaded Amplifiers	8–30
8.8	Summary	8–32
8.9	Exercises	8–34
8.10	Solutions to End–of–Chapter Exercises.....	8–37

MATLAB Scripts

Pages 8–8, 8–23, 8–43

9

Tuned Amplifiers

9.1	Introduction to Tuned Circuits	9–1
9.2	Single-tuned Transistor Amplifier.....	9–8
9.3	Cascaded Tuned Amplifiers	9–13
9.3.1	Synchronously Tuned Amplifiers.....	9–14
9.3.2	Stagger–Tuned Amplifiers	9–17
9.3.3	Three or More Tuned Amplifiers Connected in Cascade.....	9–26
9.4	Summary	9–27
9.5	Exercises	9–29
9.6	Solutions to End–of–Chapter Exercises.....	9–30

MATLAB Script

Page 9–17

10

Sinusoidal Oscillators

10.1	Oscillators Defined.....	10–1
10.2	Sinusoidal Oscillators.....	10–1
10.3	RC Oscillator.....	10–4
10.4	LC Oscillator	10–5
10.5	Armstrong Oscillator.....	10–6
10.6	Hartley Oscillator	10–7
10.7	Colpitts Oscillator	10–7
10.8	Crystal Oscillators	10–8
10.9	Pierce Oscillator	10–10
10.10	Summary.....	10–12

10.11 Exercises	10–14
10.12 Solutions to End-of-Chapter Exercises	10–15

A Introduction to MATLAB®

A.1 MATLAB® and Simulink®	A–1
A.2 Command Window	A–1
A.3 Roots of Polynomials	A–3
A.4 Polynomial Construction from Known Roots	A–4
A.5 Evaluation of a Polynomial at Specified Values	A–6
A.6 Rational Polynomials	A–8
A.7 Using MATLAB to Make Plots	A–10
A.8 Subplots	A–18
A.9 Multiplication, Division and Exponentiation	A–18
A.10 Script and Function Files	A–26
A.11 Display Formats	A–31

MATLAB Scripts

Pages A–3 through A–9, A–11 through A–13, A–16,
A–17 through A–21, A–23, A–24, A–26, A–27

B Introduction to Simulink®

B.1 Simulink and its Relation to MATLAB	B–1
B.2 Simulink Demos	B–20

MATLAB Script

Page B–4

Simulink/SimPowerSystems/SimElectronics Models

Pages B–12, B–17, B–19

C Introduction to Simscape®

C.1 Simscape Libraries	C–1
C.1.1 Foundation Library	C–1
C.1.2 Utilities Library	C–3
C.1.3 SimElectronics Library	C–4
C.1.4 SimPowerSystems Library	C–7

Simulink/SimPowerSystems/SimElectronics Model

Page C–4

D Proportional–Integral–Derivative (PID) Controller

D.1 Description and Components of a Typical PID	D–1
D.2 The Simulink PID Blocks	D–2

Simulink/SimPowerSystems/SimElectronics Models

Pages D–3, D–4

E	Compensated Attenuators	
E.1	Uncompensated Attenuator	E-1
E.2	Compensated Attenuator.....	E-2
F	Substitution, Reduction, and Miller's Theorems	
F.1	Substitution Theorem.....	F-1
F.2	Reduction Theorem.....	F-6
F.3	Miller's Theorem.....	F-10
References		R-1
Index		IN-1

1.4 Bandwidth and Frequency Response

Like electric filters, amplifiers exhibit a band of frequencies over which the output remains nearly constant. Consider, for example, the magnitude of the output voltage $|V_{\text{out}}|$ of an electric or electronic circuit as a function of radian frequency ω as shown in Figure 1.5.

As shown in Figure 1.5, the *bandwidth* is $\text{BW} = \omega_2 - \omega_1$ where ω_1 and ω_2 are the *cutoff frequencies*. At these frequencies, $|V_{\text{out}}| = \sqrt{2}/2 = 0.707$ and these two points are known as the *3-dB down* or *half-power points*. They derive their name from the fact that since power $p = v^2/R = i^2 \cdot R$, for $R = 1$ and for v or $i = \sqrt{2}/2 = 0.707$ the power is $1/2$, that is, it is “halved”.

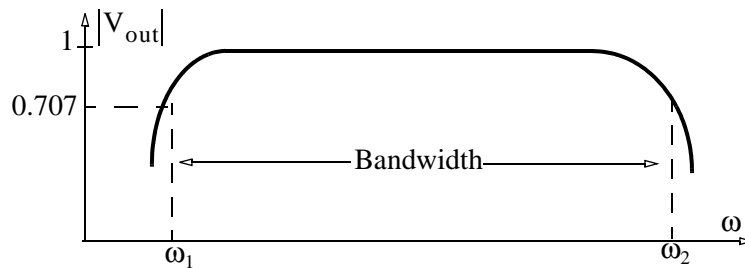


Figure 1.5. Definition of bandwidth

Alternately, we can define the bandwidth as the frequency band between half-power points. We recall from the characteristics of electric filters, the low-pass and high-pass filters have only one cut-off frequency whereas band-pass and band-elimination (band-stop) filters have two. We may think that low-pass and high-pass filters have also two cutoff frequencies where in the case of the low-pass filter the second cutoff frequency is at $\omega = 0$ while in a high-pass filter it is at $\omega = \infty$.

We also recall also that the output of circuit is dependent upon the frequency when the input is a sinusoidal voltage. In general form, the output voltage is expressed as

$$V_{\text{out}}(\omega) = |V_{\text{out}}(\omega)|e^{j\phi(\omega)} \quad (1.12)$$

where $|V_{\text{out}}(\omega)|$ is known as the *magnitude response* and $e^{j\phi(\omega)}$ is known as the *phase response*. These two responses together constitute the *frequency response* of a circuit.

Example 1.1

Derive and sketch the magnitude and phase responses of the RC low-pass filter shown in Figure 1.6.

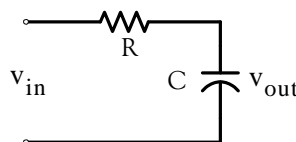


Figure 1.6. RC low-pass filter

Chapter 1 Basic Electronic Concepts and Signals

From Figure 1.16 we observe that all poles, denoted as \times , lie on the left-hand half-plane and thus the system is stable. The location of the zeros, denoted as \circ , is immaterial.

- b. We use the MATLAB **expand(s)** symbolic function to express the numerator and denominator of $G(s)$ in polynomial form

```
syms s; n=expand((s-1)*(s^2+2*s+5)), d=expand((s+2)*(s^2+6*s+25))
n = s^3+s^2+3*s-5
d = s^3+8*s^2+37*s+50
and thus
```

$$G(s) = \frac{3(s^3 + s^2 + 3s - 5)}{(s^3 + 8s^2 + 37s + 50)}$$

For this example we are interested in the magnitude only so we will use the script

```
num=3*[1 1 3 -5]; den=[1 8 37 50]; sys=tf(num,den);...
w=logspace(0,2,100); bodemag(sys,w); grid
```

The magnitude plot is shown in Figure 1.17.

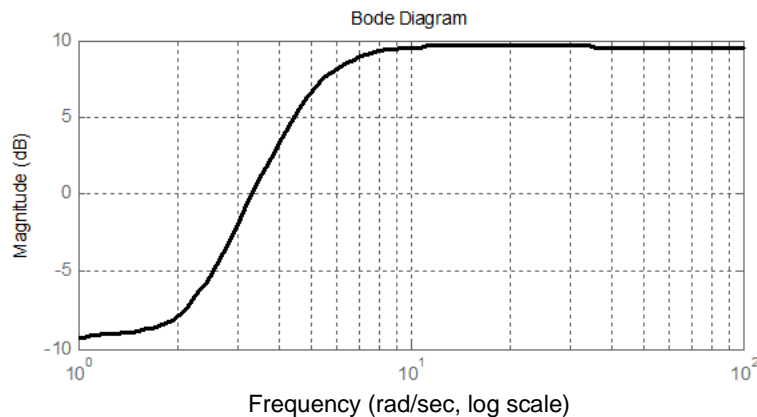


Figure 1.17. Bode plot for Example 1.3

Example 1.4

It is known that a voltage amplifier has a frequency response of a low-pass filter, a DC gain of 80 dB, attenuation of -20 dB per decade, and the 3 dB cutoff frequency occurs at 10 KHz. Determine the gain (in dB) at the frequencies 1 KHz, 10 KHz, 100KHz, 1 MHz, 10 MHz, and 100 MHz.

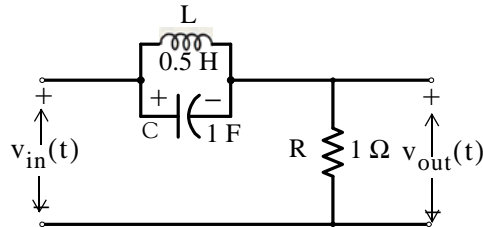
Solution:

Using the given data we construct the asymptotic magnitude response shown in Figure 1.18 from which we obtain the data shown on the table below.

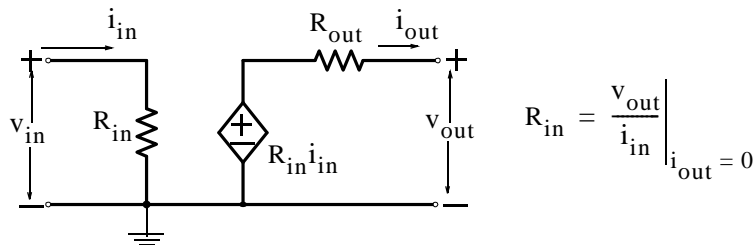
Chapter 1 Basic Electronic Concepts and Signals

1.12 Exercises

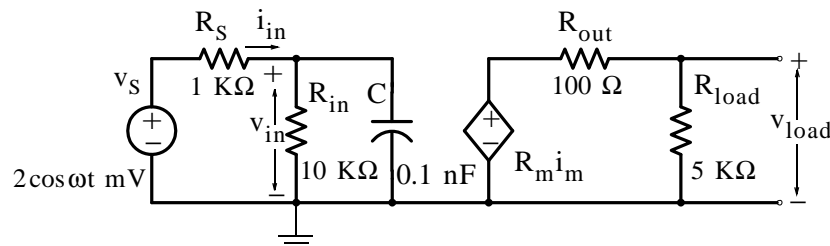
- Following the procedure of Example 1.1, derive and sketch the magnitude and phase responses for an RC high-pass filter.
- Derive the transfer function $G(s)$ for the network shown below.



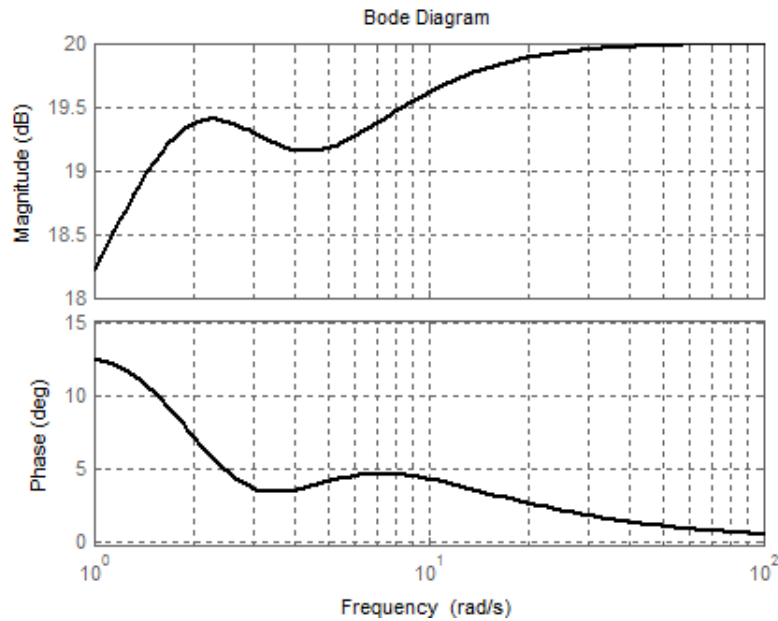
- A system has poles at -4 , $-2 + j$, $-2 - j$, and zeros at -1 , $-3 + j2$, and $-3 - j2$. Derive the transfer function of this system given that $G(\infty) = 10$.
- The circuit model shown below is known as a *transresistance amplifier* and the ideal characteristics for this amplifier are $R_{in} \rightarrow 0$ and $R_{out} \rightarrow 0$.



With a voltage source v_s in series with resistance R_s connected on the input side and a load resistance R_{load} connected to the output, the circuit is as shown below.

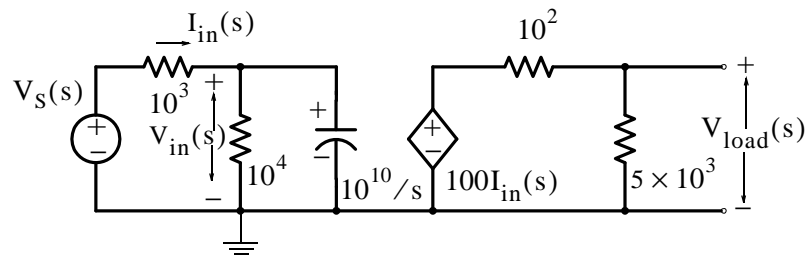


Find the overall voltage gain $A_v = v_{load}/v_s$ if $R_m = 100 \Omega$. Then, use MATLAB to plot the magnitude of A_v for the range $10^3 \leq \omega \leq 10^8$. From the plot, estimate the 3 dB cutoff frequency.



4.

The s – domain equivalent circuit is shown below.



The parallel combination of the 10^4 resistor and $10^{10}/s$ capacitor yields

$$Z(s) = 10^4 \parallel 10^{10}/s = \frac{10^{14}/s}{10^4 + 10^{10}/s} = \frac{10^{14}}{10^4 s + 10^{10}}$$

and by the voltage division expression

$$V_{in}(s) = \frac{10^{14}/(10^4 s + 10^{10})}{10^3 + 10^{14}/(10^4 s + 10^{10})} V_S(s) = \frac{10^{14}}{10^7 s + 1.1 \times 10^{14}} V_S(s)$$

Also,

$$V_{load}(s) = \frac{5 \times 10^3}{10^2 + 5 \times 10^3} 100I_{in}(s) = \frac{5 \times 10^5}{5.1 \times 10^3} I_{in}(s) = 98I_{in}(s) \quad (1)$$

where

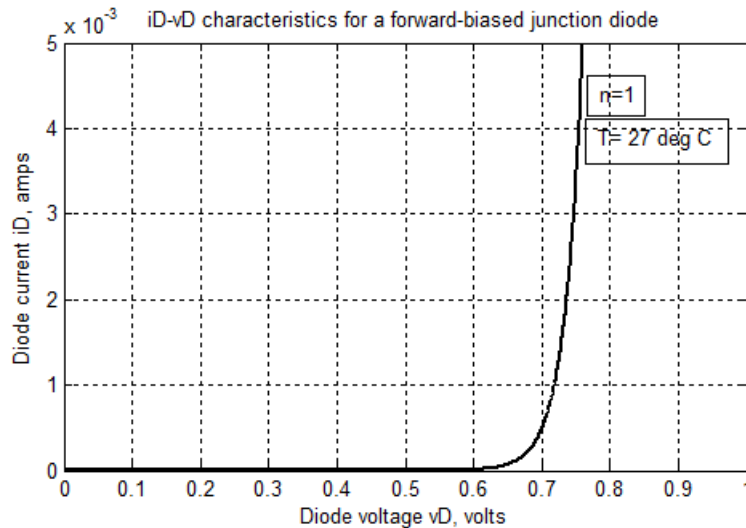


Figure 2.12. Voltage–current characteristics of a forward–biased junction diode.

The curve in Figure 2.12 shows that in a junction diode made with silicon and an impurity, conventional current will flow in the direction of the arrow of the diode as long as the voltage drop v_D across the diode is about 0.65 volt or greater. We also observe that at $v_D = 0.7 \text{ V}$, the current through the diode is $i_D \approx 0.5 \text{ mA}$.

When a junction diode is reverse–biased, as shown in Figure 2.13, a very small current will flow and if the applied voltage exceeds a certain value the diode will reach its *avalanche* or *Zener region*. The voltage–current characteristics of a reverse biased junction diode are shown in Figure 2.13 where V_Z is referred to as the Zener diode voltage. Zener diodes are discussed in the next section.

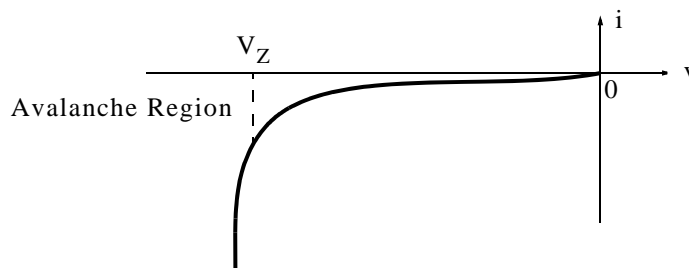


Figure 2.13. The reverse biased region of a junction diode

Commercially available diodes are provided with a given rating (volts, watts) by the manufacturer, and if these ratings are exceeded, the diode will burn–out in either the forward–biased or the reverse–biased direction.

The maximum amount of average current that can be permitted to flow in the forward direction is referred to as the *maximum average forward current* and it is specified at a special temperature, usually $25 \text{ }^\circ\text{C}$. If this rating is exceeded, structure breakdown can occur.

The maximum peak current that can be permitted to flow in the forward direction in the form of recurring pulses is referred to as the *peak forward current*.

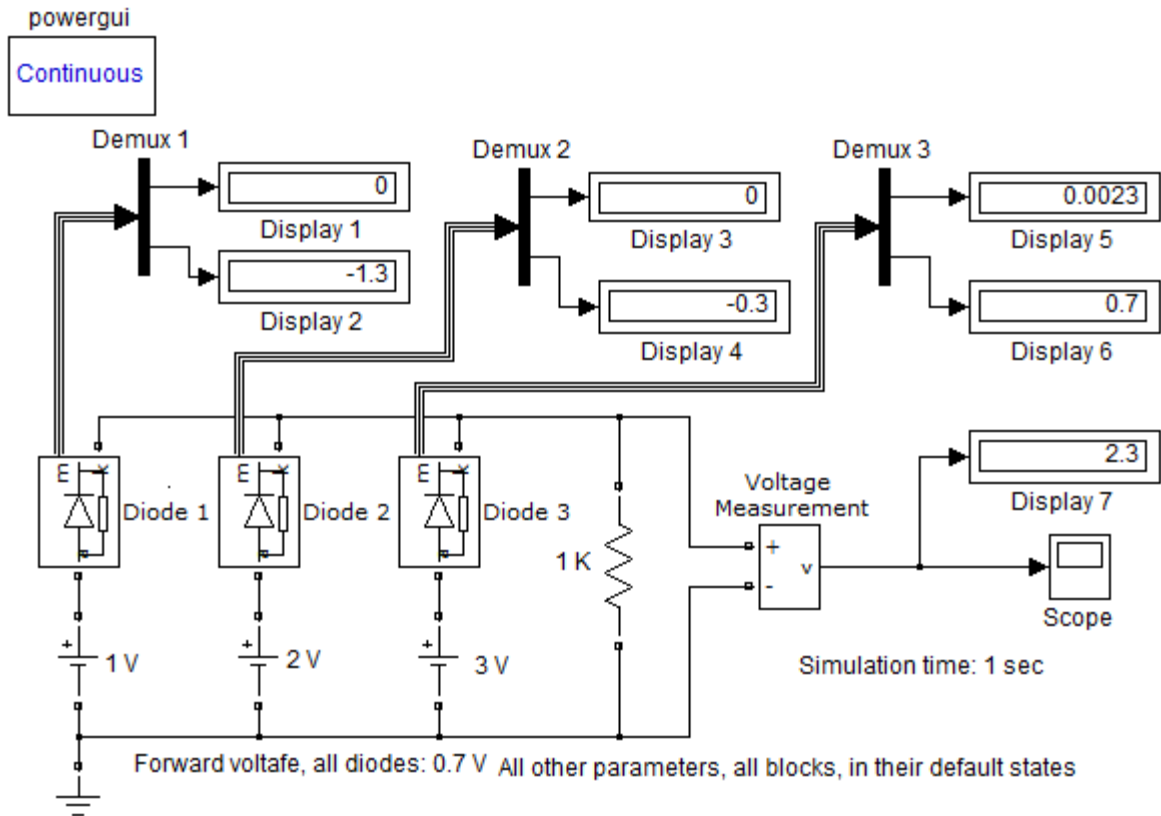


Figure 2.23. Model for Example 2.4 with SimPowerSystems blocks

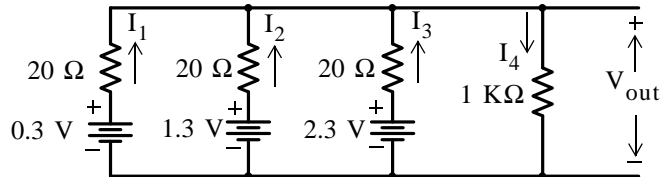


Figure 2.24. Piecewise linear equivalent circuit for Example 2.4

$$\frac{15 - 50V_{\text{out}} + 65 - 50V_{\text{out}} + 115 - 50V_{\text{out}} - V_{\text{out}}}{1000} = 0$$

This value is not consistent with the value displayed in the model in Figure 2.23, so we perform the following check:

$$I_1 \approx (0.3 - 1.3)/20 \approx -50 \text{ mA}$$

$$I_2 \approx (1.3 - 1.3)/20 \approx 0$$

$$I_3 \approx (2.3 - 1.3)/20 \approx 50 \text{ mA}$$

$$I_4 = 1.3/1000 = 1.3 \text{ mA}$$

$$I_1 + I_2 + I_3 \neq I_4$$

The minus (–) sign for the current I_1 indicates that this current flows in the opposite direction of the one shown. Also, the current I_2 is zero. Therefore, we must conclude that only the diode on the right side conducts and by the voltage division expression

$$V_{\text{out}} = \frac{1000}{20 + 1000} \times 2.3 \approx 2.3 \text{ V}$$

2.5 Low Frequency AC Circuits with Junction Diodes

When used with AC circuits of low frequencies, diodes, usually with $1.8 \leq n \leq 2.0$ are biased to operate at some point in the neighborhood of the relatively linear region of the $i - v$ characteristics where $0.65 \leq v_D \leq 0.8 \text{ V}$. A bias point denoted as Q whose coordinates are $Q(V_D, I_D)$ is shown in Figure 2.25 for a junction diode with $n = 2$.

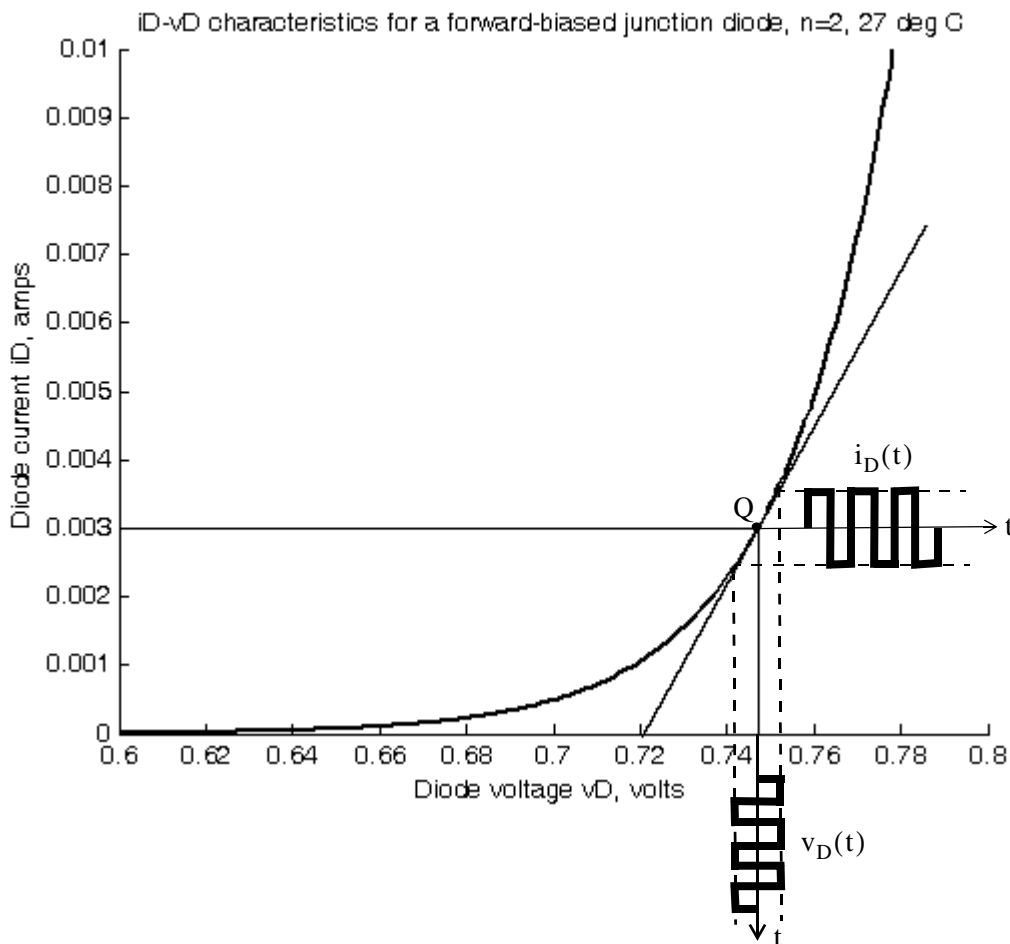


Figure 2.25. Junction diode biased at point Q and changes in i_D corresponding to changes in v_D

Figure 2.25 shows how changes in $v_D(t)$ result in changes in $i_D(t)$.

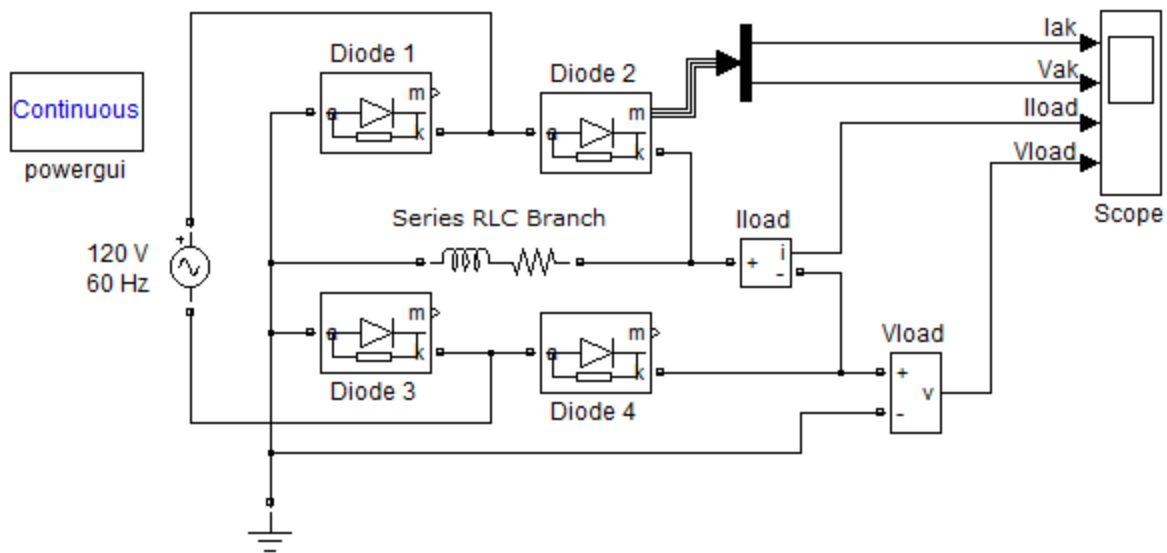


Figure 2.40. Simulation of a full-wave rectifier with SimPower Toolbox

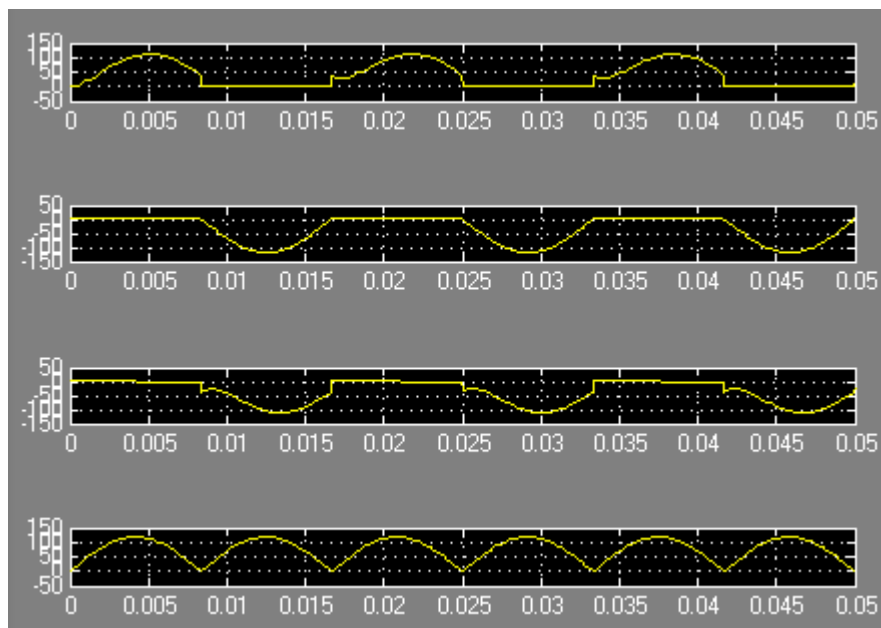
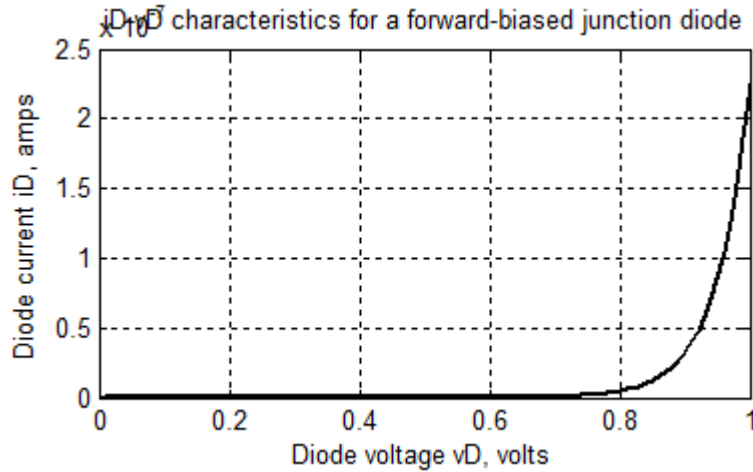


Figure 2.41. Waveforms displayed in the Scope block in Figure 2.40

2.20 Solutions to End-of-Chapter Exercises

1. `vD=0: 0.01: 1; iR=10^(-15); n=2; VT=26*10^(-3); iD=iR.*(exp(vD./(n.*VT))-1); plot(vD,iD);...
 xlabel('Diode voltage vD, volts'); ylabel('Diode current iD, amps');...
 title('iD-vD characteristics for a forward-biased junction diode'); grid`



We observe that when $n = 2$, the diode begins to conduct at approximately 7.8 V.

2. Let $I_{D1} = I_s e^{V_{D1}/nV_T}$ and $I_{D2} = I_s e^{V_{D2}/nV_T}$. Then,

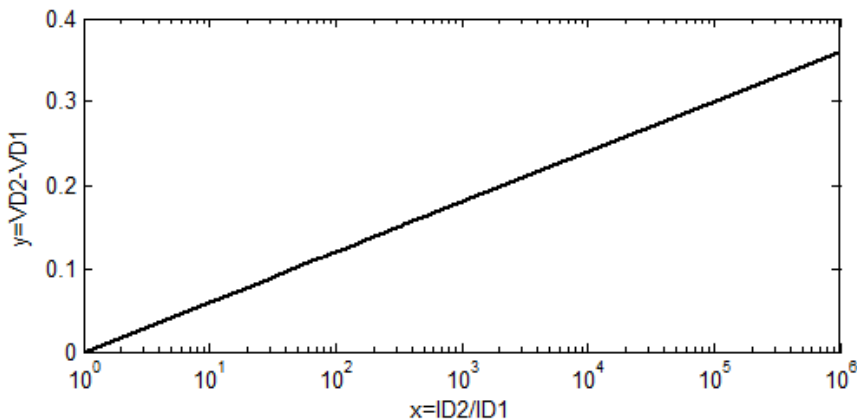
$$I_{D2}/I_{D1} = e^{V_{D2}/nV_T} / e^{V_{D1}/nV_T} = e^{(V_{D2} - V_{D1})/nV_T}$$

or

$$V_{D2} - V_{D1} = nV_T \ln(I_{D2}/I_{D1}) = 2.3nV_T \log_{10}(I_{D2}/I_{D1})$$

For convenience, we let $V_{D2} - V_{D1} = y$ and $I_{D2}/I_{D1} = x$ and we use the following MATLAB script to plot $y = 2.3nV_T \log_{10}x$ on semilog scale.

`x=1: 10: 10^6; y=2.3.*1.*26.*10.^(-3).*log10(x); semilogx(x,y);...
 xlabel('x=ID2/ID1'); ylabel('y=VD2-VD1')`



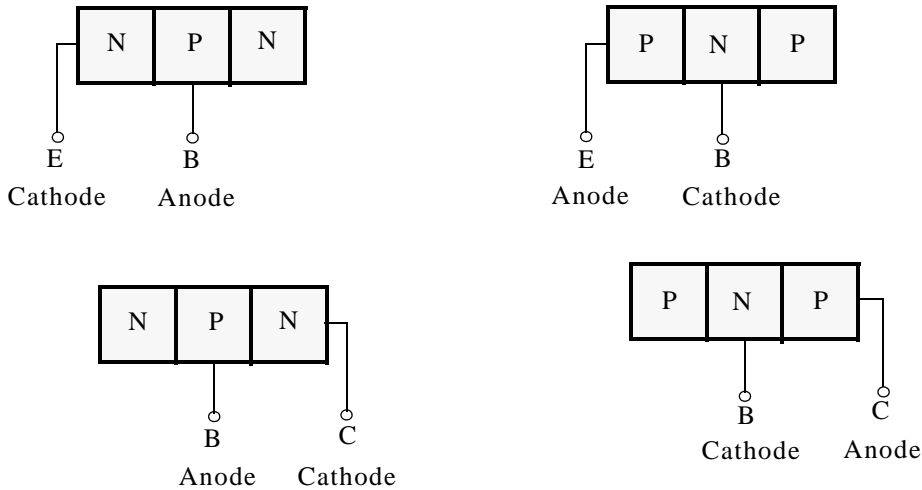


Figure 3.2. Transistors configured as diodes

Transistors are used either as amplifiers or more commonly as electronic switches. We will discuss these topics on the next section. Briefly, a typical NPN transistor will act as a closed switch when the voltage V_{BE} between its base and emitter terminals is greater than 0.7 V but no greater than 5 V to avoid possible damage. The transistor will act as an open switch when the voltage V_{BE} is less than 0.6 V. Figure 3.3 shows an NPN transistor used as an electronic switch to perform the operation of inversion, that is, the transistor inverts (changes) an input of 5 V to an output of 0 V when it behaves like a closed switch as in Figure 3.3, and it inverts an input of 0 V to an output of 5 V when it behaves like an open switch as in Figure 3.4.

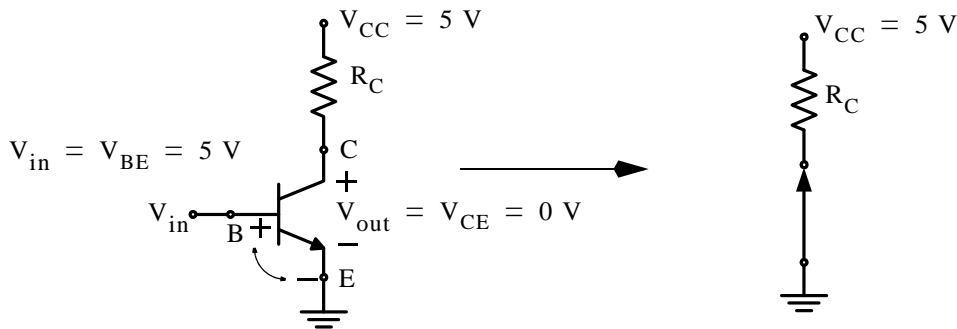


Figure 3.3. NPN transistor as electronic closed switch – inverts 5 V to 0 V

Like junction diodes, most transistors are made of silicon. Gallium Arsenide (GaAs) technology has been under development for several years and its advantage over silicon is its speed, about six times faster than silicon, and lower power consumption. The disadvantages of GaAs over silicon is that arsenic, being a deadly poison, requires very special manufacturing processes and, in addition, it requires special handling since it is extremely brittle. For these reasons, GaAs is much more expensive than silicon and it is usually used only in superfast computers.

$$e^{v_{BE}/V_T} = \frac{5 \times 10^{-6}}{10^{-16}} = 5 \times 10^{10}$$

$$v_{BE}/V_T = \ln(5 \times 10^{10})$$

$$v_{BE} = V_T(\ln 5 + 10 \ln 10) = 26 \times 10^{-3}(1.61 + 23.03) \approx 0.64 \text{ V}$$

The collector bias voltage V_{CC} is used for proper transistor operation and its value is not required for the above calculations.

3.3.2 Equivalent Circuit Models – PNP Transistors

Relations (3.15), (3.16), and (3.17) apply also to PNP transistor equivalent circuits except that v_{BE} needs to be replaced by v_{EB} as shown in Figure 3.8.

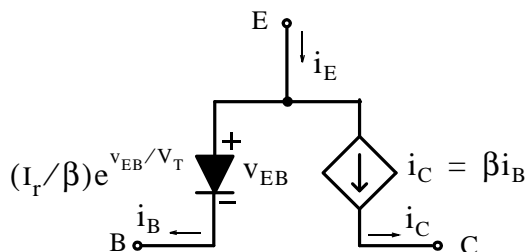


Figure 3.8. PNP transistor equivalent circuit model for relations (3.15), (3.16), and (3.17)

For easy reference we summarize the current–voltage relationships for both NPN and PNP transistors in the active mode in Table 3.1.

TABLE 3.1 NPN and PNP transistor current–voltage characteristics

NPN Transistor			PNP Transistor		
$\alpha = \frac{\beta}{\beta + 1} = \frac{i_C}{i_E}$	$\beta = \frac{\alpha}{1 - \alpha} = \frac{i_C}{i_B}$	$i_E = i_B + i_C$	$\alpha = \frac{\beta}{\beta + 1} = \frac{i_C}{i_E}$	$\beta = \frac{\alpha}{1 - \alpha} = \frac{i_C}{i_B}$	$i_E = i_B + i_C$
$i_B = \left(\frac{I_r}{\beta}\right)e^{\frac{v_{BE}}{V_T}}$	$i_C = I_r e^{\frac{v_{BE}}{V_T}}$	$i_E = \left(\frac{I_r}{\alpha}\right)e^{\frac{v_{BE}}{V_T}}$	$i_B = \left(\frac{I_r}{\beta}\right)e^{\frac{v_{EB}}{V_T}}$	$i_C = I_r e^{\frac{v_{EB}}{V_T}}$	$i_E = \left(\frac{I_r}{\alpha}\right)e^{\frac{v_{EB}}{V_T}}$
$i_B = i_C/\beta$	$i_C = \beta i_B$	$i_B = i_C/\alpha$	$i_B = i_C/\beta$	$i_C = \beta i_B$	$i_B = i_C/\alpha$
$i_B = i_E/(\beta + 1)$	$i_C = \alpha i_E$	$i_E = (\beta + 1)i_B$	$i_B = i_E/(\beta + 1)$	$i_C = \alpha i_E$	$i_E = (\beta + 1)i_B$
$i_B = (1 - \alpha) i_E$	$V_T = 26 \text{ mV at } T = 27^\circ \text{C}$		$i_B = (1 - \alpha) i_E$	$V_T = 26 \text{ mV at } T = 27^\circ \text{C}$	
$v_{BE} = V_T [\ln(\beta) - \ln(I_r) + \ln(i_B)]$			$v_{BE} = V_T [\ln(\beta) - \ln(I_r) + \ln(i_B)]$		

The relations in Table 3.1 are very useful in establishing voltage and current levels at various points on an NPN or PNP transistor.

Chapter 3 Bipolar Junction Transistors

mode are provided by the transistor manufacturers. Please refer to the last section in this chapter. Table 3.3 lists the h -parameter equations for the three bipolar transistor configurations.

TABLE 3.3 h -parameter equations for transistors

Parameter	Common-Base	Common-Emitter	Common-Collector
h_{11}	h_{ib}	$h_{ie} \approx h_{11}/(1 + h_{21})$	$h_{ic} \approx h_{11}/(1 + h_{21})$
h_{12}	h_{rb}	$h_{re} \approx h_{11}h_{22}/(1 + h_{21}) - h_{12}$	$h_{rc} \approx 1$
h_{21}	h_{fb}	$h_{fe} \approx -h_{21}/(1 + h_{21})$	$h_{fc} \approx -1/(1 + h_{21})$
h_{22}	h_{ob}	$h_{oe} \approx h_{22}/(1 + h_{21})$	$h_{oc} \approx h_{22}/(1 + h_{21})$

Example 3.15

For the amplifier circuit in Figure 3.62 it is known that $r_n = h_{11} = 2 \text{ K}\Omega$, $\beta = h_{21} = 100$, $\mu = h_{12} = 5 \times 10^{-4}$, and $g_o = h_{22} = 2 \times 10^{-5} \text{ }\Omega^{-1}$. Find the small signal current amplification $A_c = i_{\text{load}}/i_s$.

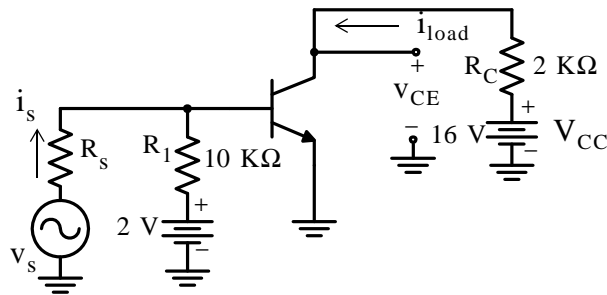


Figure 3.62. Transistor amplifier for Example 3.15

Solution:

The incremental model of this transistor amplifier is shown in Figure 3.63 where

$$R_{eq} = \frac{(1/g_o)R_{load}}{1/g_o + R_{load}} = \frac{50 \times 10^3 \times 2 \times 10^3}{52 \times 10^3} = 1.923 \text{ K}\Omega$$

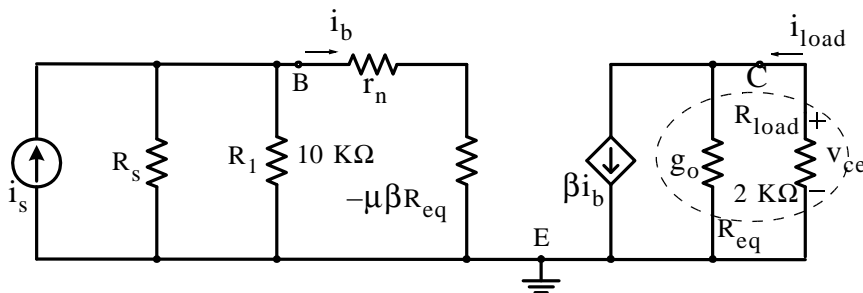


Figure 3.63. The incremental model for the transistor circuit in Figure 3.62

$$g_m = \frac{\partial I_C}{\partial V_B} = \frac{1}{V_T} \cdot \underbrace{I_S(e^{(V_B - V_E)/V_T})}_{I_C} \quad (3.185)$$

or

$$g_m = \frac{I_C}{V_T} \quad (3.186)$$

Using the relations

$$I_C = \beta_F I_B = \alpha_F I_E \quad I_E = \frac{I_C}{\alpha_F} = (\beta_F + 1) I_B \quad I_B = \frac{I_C}{\beta_F} = \frac{I_E}{\beta_F + 1} \quad (3.187)$$

we can also express these small-signal parameters in terms of one another as

$$r_b = \frac{\beta_F}{g_m} = (\beta_F + 1) r_e \quad r_e = \frac{\alpha_F}{g_m} = \frac{r_b}{\beta_F + 1} \quad g_m = \frac{\beta_F}{r_b} = \frac{\alpha_F}{r_e} \quad (3.188)$$

3.5 Schottky Diode Clamp

In the saturation region, the collector–base diode is forward-biased. Due to the large diffusion capacitance, it takes a considerably long time to drive the transistor out of saturation. The *Schottky diode* alleviates this problem if connected between the base and the collector as shown in Figure 3.88.

The Schottky diode has the property that it turns on at a lower voltage than the PN junction. Therefore, when a transistor is in the saturation region, the current between the base and the collector is carried by the Schottky diode.

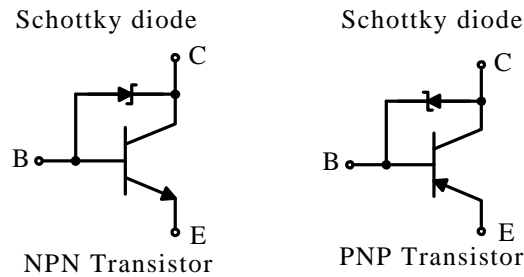
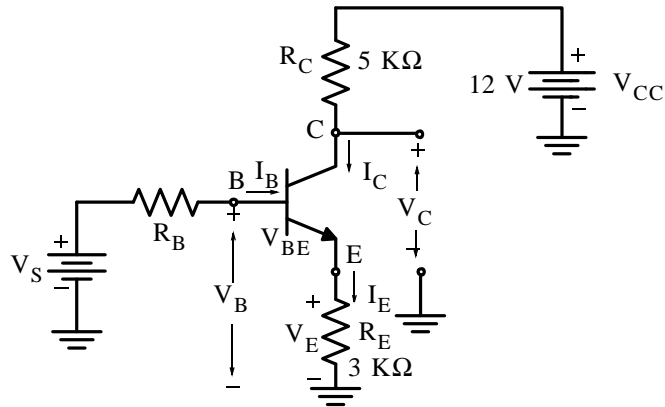


Figure 3.88. NPN and PNP transistors with Schottky diodes

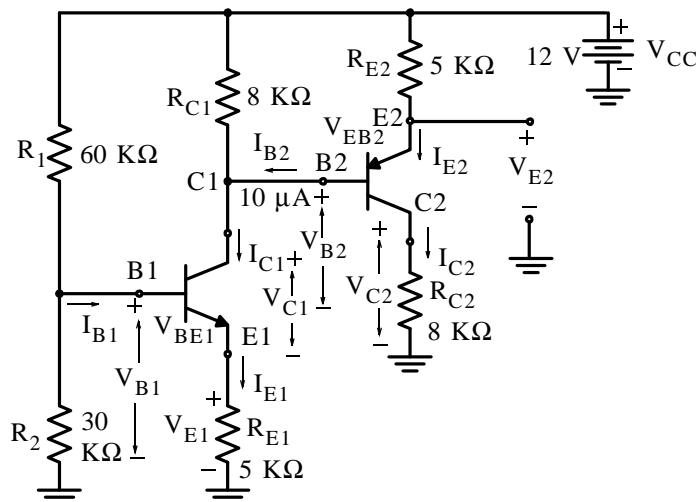
3.6 Transistor Specifications

Transistors are available in a variety of shapes and sizes, each with its own unique characteristics. The specifications usually cover the items listed below, and the values given are typical.

1. Features, e.g., NPN Silicon Epitaxial Planar Transistor for switching and amplifier applications, and mechanical data, e.g., case, weight, and packaging options.



9. For an NPN transistor circuit $\beta = 100$, $V_{CC} = 11.3 \text{ V}$, $V_B = 3.5 \text{ V}$ and with the reverse-biased collector–base junction set at $V_{CB} = 1.8 \text{ V}$ we want the collector current to be $I_C = 0.8 \text{ mA}$. What should the values of R_C and R_E be to achieve this value?
10. For a PNP transistor circuit with $\beta = 120$, $V_{EE} = 12 \text{ V}$, $V_B = 0 \text{ V}$, $V_{CC} = -12 \text{ V}$, and $R_E = 3 \text{ K}\Omega$, what would the largest value of R_C be so that the transistor operates at the active mode?
11. For a PNP transistor circuit with $\beta = 150$, $V_{EE} = 12 \text{ V}$, $V_B = 0 \text{ V}$, $V_{CC} = -12 \text{ V}$, $I_E = 0.8 \text{ mA}$, and $V_{CB} = -3 \text{ V}$, what should the values of R_C and R_E be so that the transistor operates at the active mode?
12. For the circuit below, it is known that $\beta = 120$ for both transistors. Find all indicated voltages and currents. Are both the transistors operating in the active mode? What is the total power absorbed by this circuit?



Chapter 4

Field Effect Transistors and PNP Devices

This chapter begins with a discussion of Field Effect Transistors (FETs), characteristics, and applications. Other PNP devices, the four-layer diode, the silicon controlled rectifier (SCR), the silicon controlled switch (SCS), and the triac are introduced with some of their applications. The chapter includes also a brief discussion on unijunction transistors, and diacs.

4.1 Junction Field Effect Transistor (JFET)

The *Field-Effect Transistor* (FET) is another semiconductor device. The Junction FET (JFET) is the earlier type and the *Metal Oxide Semiconductor* FET (MOSFET) is now the most popular type. In this section we will discuss the JFET and we will discuss the MOSFET in the next section.

Figure 4.1(a) shows the basic JFET amplifier configuration and the output volt-ampere characteristics are shown in Fig. 4.1(b). These characteristics are similar to those for the junction transistor except that the parameter for this family is the input voltage rather than the input current. Like the old vacuum triode, the FET is a voltage-controlled device.

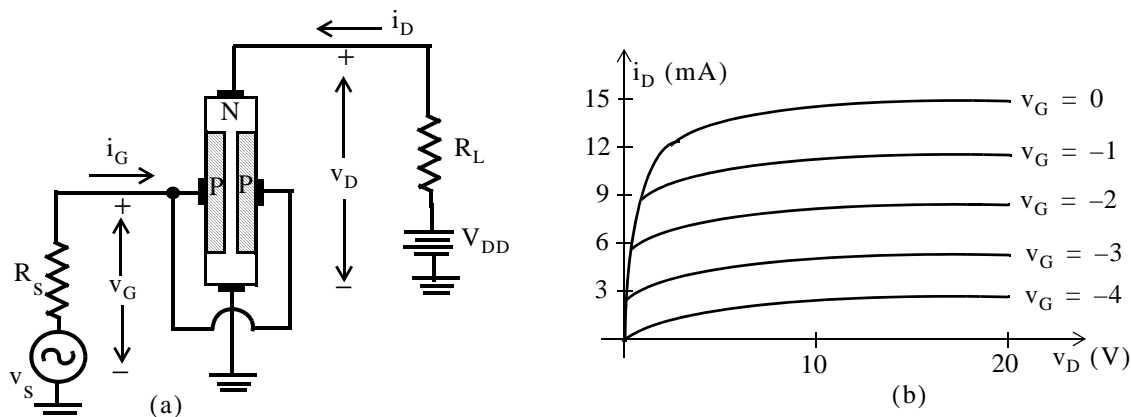


Figure 4.1. Pictorial representation and output volt-ampere characteristics for a typical JFET

The lower terminal in the N material is called the *source*, and the upper terminal is called the *drain*; the two regions of P material, which are usually connected together externally, are called *gates*. P-N junctions exist between the P and N materials, and in normal operation the voltage applied to the gates biases these junctions in the reverse direction. A potential barrier exists across the junctions, and the electrons carrying the current i_D in the N material are forced to flow through the channel between the two gates. If the voltage applied to the gates is changed, the width of the transition region at the junction changes; thus the width of the channel changes, resulting in a change in the resistance between source and drain. In this way the current in the output circuit is controlled by the gate voltage. A small potential applied to the gates, 5 to 10 volts, is sufficient to reduce the channel width to zero and to cut off the flow of current in the output circuit.

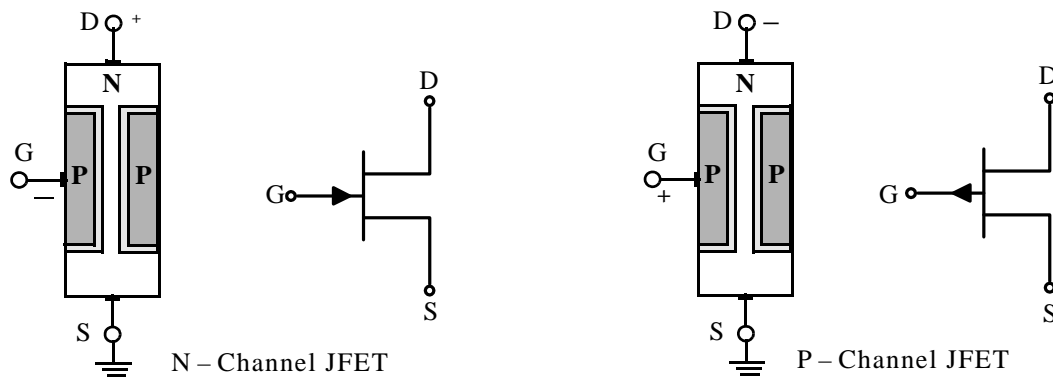


Figure 4.4. N-Channel and P-Channel JFETs

Like in bipolar transistors, one important parameter in FETs is its *transconductance* g_m defined as the ratio of the change in current i_{DS} to the change of voltage v_{GS} which produced it. In other words,

$$g_m = \left. \frac{\partial i_{DS}}{\partial v_{GS}} \right|_{v_{DS} = \text{constant}} \quad (4.1)$$

Example 4.1

Figure 4.5 shows a common-source N-channel JFET amplifier circuit and Table 4.1 shows several values of the current i_{DS} corresponding to the voltage v_{GS} .

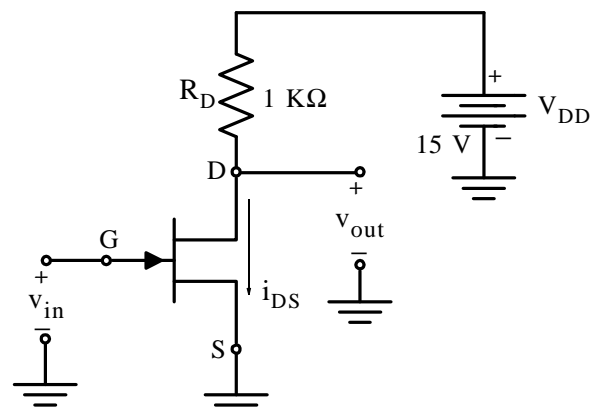


Figure 4.5. Common-source N-channel JFET amplifier for Example 4.1

TABLE 4.1 Current i_{DS} versus voltage v_{GS} for Example 4.1

v_{GS} (V)	0	-1	-2	-3	-4
i_{DS} (mA)	35	20	8	2	0

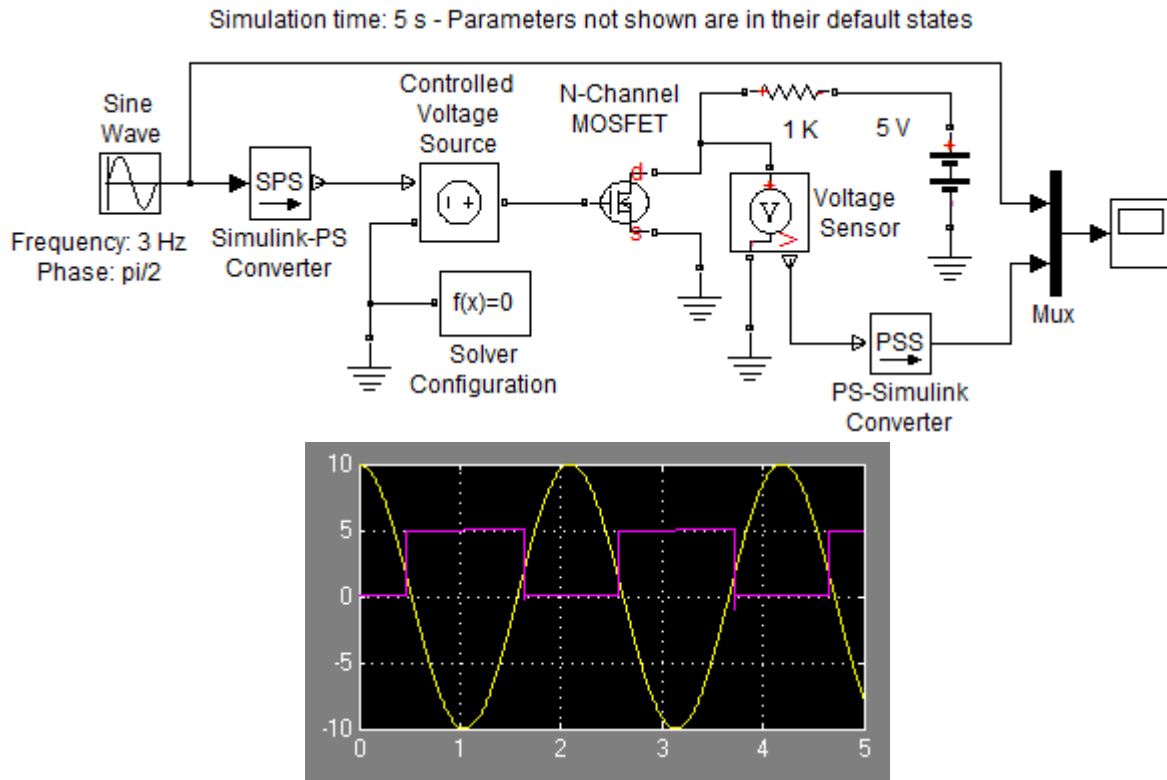


Figure 4.13. SimElectronics model with an N-Channel MOSFET

Relation (4.8) which is repeated below for convenience, represents an n – channel MOSFET and we observe that, in saturation, the drain current i_D is independent of the drain voltage v_{DS}

$$i_D = \frac{1}{2} \cdot k_n \frac{W}{L} (v_{GS} - V_T)^2 \quad \text{for } v_{DS} \geq v_{GS} - V_T \quad (4.11)$$

Therefore, we conclude that in the saturation mode the n – channel MOSFET behaves as an ideal current source whose value is as in (4.11).

In analogy with the transconductance in bipolar junction transistors, the MOSFET *transconductance* is defined as

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{DS} = \text{constant}} \quad (4.12)$$

In other words, the transconductance is a measure of the sensitivity of drain current to changes in gate-to-source bias.

As indicated in the previous chapter, subscripts in upper case represent the sum of the quiescent and small signal parameters, and subscripts in lower case represent just the small signal parameters. Thus, $v_{GS} = V_{GS} + v_{gs}$ and (4.11) can be expressed as

Note 1: In the inverting mode, the resistor R connected between the non-inverting (+) input and ground serves only as a current limiting device, and thus it does not influence the op amp's gain. So its presence or absence in an op amp circuit is immaterial.

Note 2: The input voltage v_{in} and the output voltage v_{out} as indicated in the circuit of Figure 5.3, should not be interpreted as open circuits; these designations imply that an input voltage of any waveform may be applied at the input terminals and the corresponding output voltage appears at the output terminals.

As shown in the relation of (5.1), the gain for this op amp configuration is the ratio $-R_f/R_{in}$ where R_f is the feedback resistor which allows portion of the output to be fed back to the input. The minus (-) sign in the gain ratio $-R_f/R_{in}$ implies that the output signal has opposite polarity from that of the input signal; hence the name inverting amplifier. Therefore, when the input signal is positive (+) the output will be negative (-) and vice versa. For example, if the input is +1 volt DC and the op amp gain is 100, the output will be -100 volts DC. For AC (sinusoidal) signals, the output will be 180° out-of-phase with the input. Thus, if the input is 1 volt AC and the op amp gain is 5, the output will be -5 volts AC or 5 volts AC with 180° out-of-phase with the input.

Example 5.1

Compute the voltage gain G_v and then the output voltage v_{out} for the inverting op amp circuit shown in Figure 5.4, given that $v_{in} = 1 \text{ mV}$. Plot v_{in} and v_{out} as mV versus time on the same set of axes.

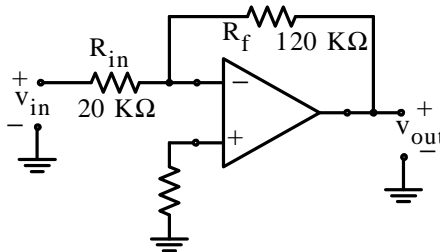


Figure 5.4. Circuit for Example 5.1

Solution:

This is an inverting amplifier and thus the voltage gain G_v is

$$G_v = -\frac{R_f}{R_{in}} = -\frac{120 \text{ K}\Omega}{20 \text{ K}\Omega} = -6$$

and since

$$G_v = v_{out}/v_{in}$$

the output voltage is

$$v_{out} = G_v v_{in} = -6 \times 1$$

or

$$v_{out} = -6 \text{ mV}$$

$$v_C = \frac{1}{C} \int_0^t i_C dt + V_0 \quad (5.43)$$

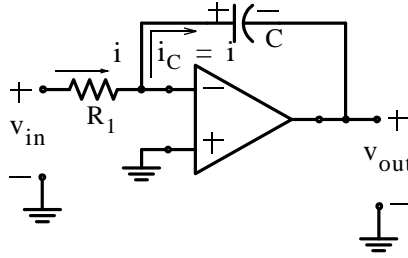


Figure 5.53. The Miller integrator

Since the inverting input is at virtual ground, the output voltage v_{out} is the negative of the capacitor voltage v_C , that is, $v_{out} = -v_C$, and thus

$$v_{out} = -\frac{1}{C} \int_0^t i_C dt - V_0 \quad (5.44)$$

Also, since

$$i_C = i = \frac{v_{in}}{R_1} \quad (5.45)$$

we rewrite (5.44) as

$$v_{out} = -\frac{1}{R_1 C} \int_0^t v_{in} dt - V_0 \quad (5.46)$$

Example 5.17

The input voltage to the amplifier in Figure 5.53(a) is as shown in Figure 5.54(b). Find and sketch the output voltage assuming that the initial condition is zero, that is, $V_0 = 0$.

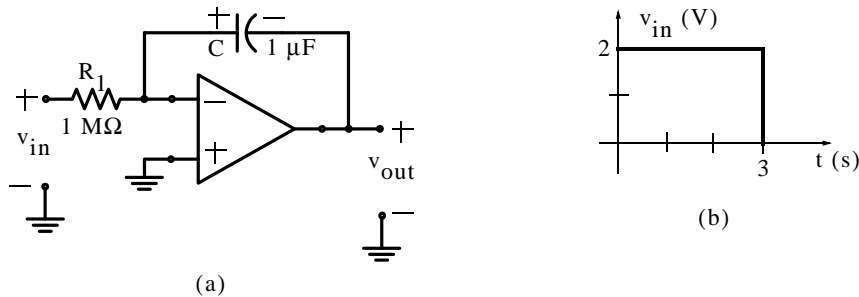


Figure 5.54. Circuit and input waveform for Example 5.17

Solution:

From relation (5.46)

$$v_{out} = -\frac{1}{R_1 C} \int_0^t v_{in} dt - V_0$$

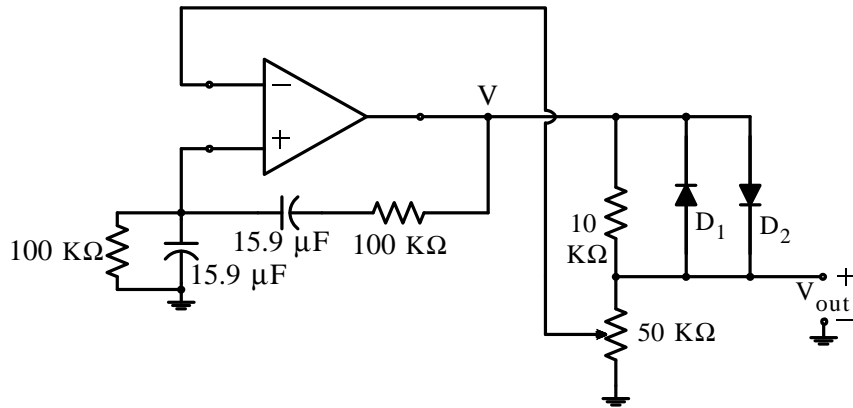


Figure 5.82. Circuit for Example 5.21

5.23 Digital-to-Analog Converters

As we will see in Chapter 6, digital systems* recognize only two levels of voltage referred to as HIGH and LOW signals or as logical 1 and logical 0. This two-level scheme works well with the binary number system. It is customary to indicate the HIGH (logical 1) and LOW (logical 0) by Single-Pole-Double-Throw (SPDT) switches that can be set to a positive non-zero voltage like 5 volts for HIGH and zero volts or ground for LOW as shown in Figure 5.83.

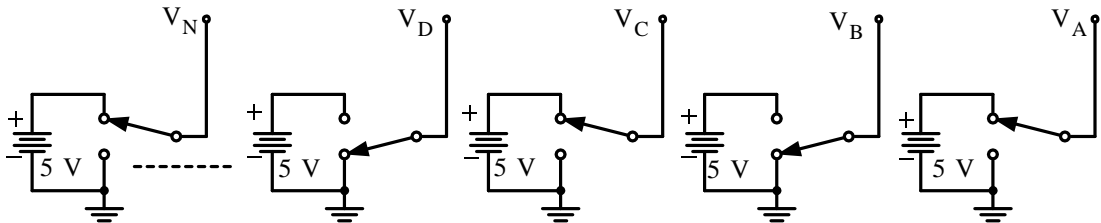


Figure 5.83. Digital circuit represented by SPDT switches

In Figure 5.81 $V_D = 0$, $V_C = 1$, $V_B = 0$, and $V_A = 1$, that is, switches A and C are HIGH (5 volts) and switches B and D are LOW (0 volts). The first 16 binary numbers representing all possible combinations of the four switches with voltage settings V_A (least significant position) through V_D (most significant position), and their decimal equivalents are shown in Table 5.1.

A digital-to-analog (D/A or DAC) converter is used to convert a binary output from a digital system to an equivalent analog voltage. If there are 16 combinations of the voltages V_D through V_A , the analog device should have 16 possible values. For example, since the binary number 1010 (decimal 10) is twice the value of the binary number 0101 (decimal 5), an analog equivalent voltage of 1010 must be double the analog voltage representing 0101.

* Refer also to *Digital Circuit Analysis and Design with Simulink Modeling and Introduction to CPLDs and FPGAs*, ISBN 978-1-934404-05-8.

Example 5.24

How many clock cycles would we need to obtain a 10-bit resolution with a dual-slope ADC?

Solution:

The integration time T_1 would require $2^{10} = 1024$ clock cycles and also another $2^{10} = 1024$ clock cycles for integration time T_2 for a maximum conversion of $2 \times 2^{10} = 2048$ clock cycles.

5.26 Op Amps in Analog Computers

Present day *analog computers* are build with op amps. In an analog computer the numbers representing the variables are voltages. We will not discuss analog computers in this section. We will simply present two simple examples to illustrate how op amps are used in analog computation.

Example 5.25

Using two op amps and resistors, design an analog computer that will solve the equations

$$\begin{aligned}a_1x + b_1y &= c_1 \\a_2x + b_2y &= c_2\end{aligned}\tag{5.74}$$

where a_1 , a_2 , b_1 , b_2 , c_1 , and c_2 are constant coefficients.

Solution:

We observe that the arithmetic operations involved in (5.74) are addition and multiplication by constant coefficients. The two additions can be performed by summing op amps. Multiplication by a coefficient greater than unity can be performed with an op amp with feedback, and if the coefficient is less than unity, we can use a voltage divider. It is convenient to express the given equations as

$$\begin{aligned}x &= \frac{c_1}{a_1} - \frac{b_1}{a_1}y \\y &= \frac{c_2}{b_2} - \frac{a_2}{b_2}x\end{aligned}\tag{5.75}$$

and these equations can be solved using two summing amplifiers as shown in Figure 5.93. As shown in Figure 5.95, the output of op amp A_1 is a voltage representing the unknown x and the output of op amp A_2 is a voltage representing the unknown y . The fraction b_1/a_1 of y is obtained from the potentiometer R_{adj4} and this is summed in op amp A_1 with the fraction $-c_1/a_1$ obtained from potentiometer R_{adj1} and voltage source V_{s1} . A similar summation is obtained by amplifier A_2 .

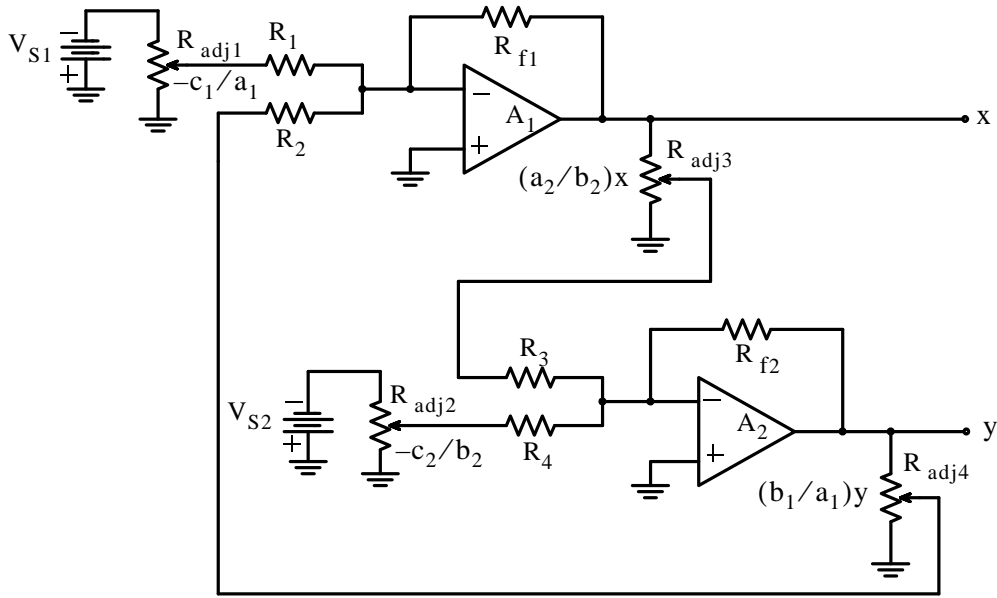


Figure 5.95. Analog computer for the solution of two simultaneous equations with two unknowns

In Figure 5.95 the scaling factors chosen must ensure that the voltages representing the unknowns do not exceed the output capability of the op amps. This procedure can be extended to the solution of simultaneous equations with more than two unknowns.

Before we consider the next example for a circuit to solve a simple differential equation, we need to discuss a practical integrator circuit that provides some means of setting a desired initial value at the beginning of the integration cycle. It is also necessary to provide means to stop the integrator at any time, and for the integrator output to remain constant at the value it has reached at that time. An integrator circuit that provides these means is shown in Figure 5.96.

Initially, the integrator sets the initial condition with the switches as shown in Figure 5.94(a), and denoting the initial condition as V_0 . The voltage across the capacitor cannot change instantaneously, and thus

$$v_{\text{out}}(t = 0) = -\frac{R_2}{R_1} V_0 \quad (5.76)$$

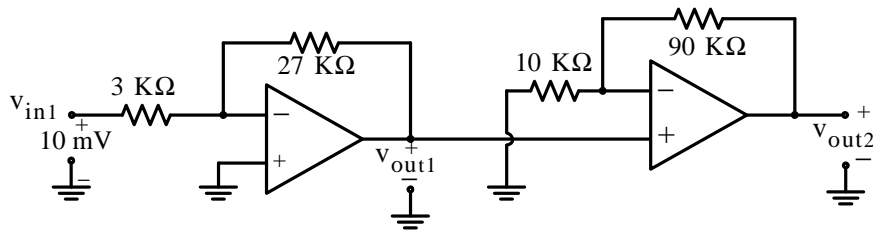
When switched to the compute mode, the circuit integrates the input voltage and the value of the output voltage is

$$v_{\text{out}} = v_{\text{out}}(t = 0) - \frac{1}{R_{\text{in}} C} \int_0^t v_{\text{in}} dt \quad (5.77)$$

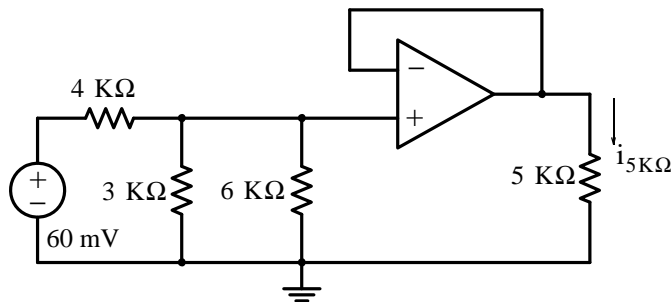
The integrator is then switched to the hold mode and remains constant at the value reached at the end of the compute mode. We observe that the switches in the hold mode are positioned as in the set initial condition mode.

5.29 Exercises

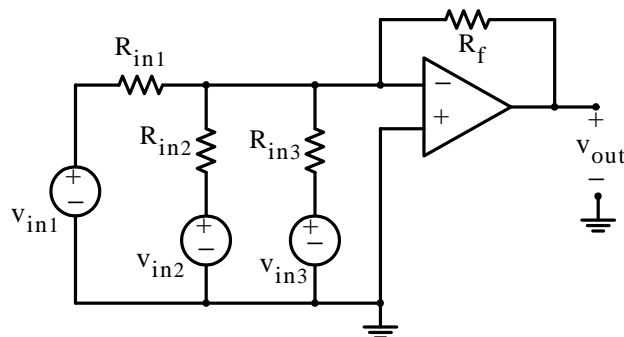
1. For the circuit below compute v_{out2} .



2. For the circuit below compute $i_{5K\Omega}$.



3. For the circuit below, R_{in1} , R_{in2} , and R_{in3} represent the internal resistances of the input voltages v_{in1} , v_{in2} , and v_{in3} respectively. Derive an expression for v_{out} in terms of the input voltage sources, their internal resistances, and the feedback resistance R_f .



This chapter begins with an introduction to electronic logic gates and their function in terms of Boolean expressions and truth tables. Positive and negative logic are defined, and the transistor–transistor logic (TTL), emitter–coupled logic (ECL), CMOS, and BiCMOS logic families are discussed. Earlier logic families are presented in the exercises section.

6.1 Basic Logic Gates^{*}

Electronic logic gates are used extensively in digital systems and are manufactured as integrated circuits (IC's). The basic logic gates are the inverter or NOT gate, the AND gate, and the OR gate, and these perform the complementation, ANDing, and ORing operations respectively. The symbols for these gates are shown in Figure 6.1.

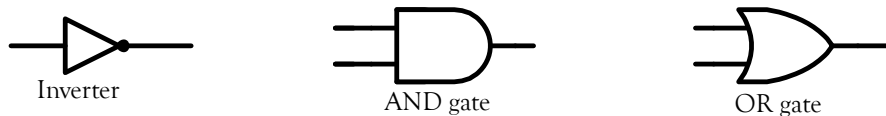


Figure 6.1. The three basic logic gates

Four other logic gates, known as NAND, NOR, Exclusive OR (XOR), and Exclusive NOR (XNOR), are derivatives of the basic AND and OR gates and will be discussed later in this chapter.

6.2 Positive and Negative Logic

Generally, an uncomplemented variable represents a logical 1, also referred to as the *true* condition, and when that variable is complemented, it represents a logical 0, also referred to as the *false* condition. Thus, if $A = 1$ (true), it follows that $\bar{A} = 0$ (false). Of course, digital computers do not understand logical 1, logical 0, true, or false; they only understand voltage signals such as that shown in Figure 6.2.



Figure 6.2. Typical voltage signal for a digital computer

With reference to the voltage waveform of Figure 6.2, integrated circuit manufacturers assign the letter H (High) to the 5 volt level and the letter L (Low) to the ground level as shown in Figure 6.3.

^{*} For this and the remaining chapters it is assumed that the reader has prior knowledge of the binary, the octal, and hexadecimal number systems, complements of numbers, binary codes, the fundamentals of Boolean algebra, and truth tables. If not, it is strongly recommended that a good book like our *Digital Circuit Analysis and Design*, ISBN 978–1–934404–05–8 is reviewed.

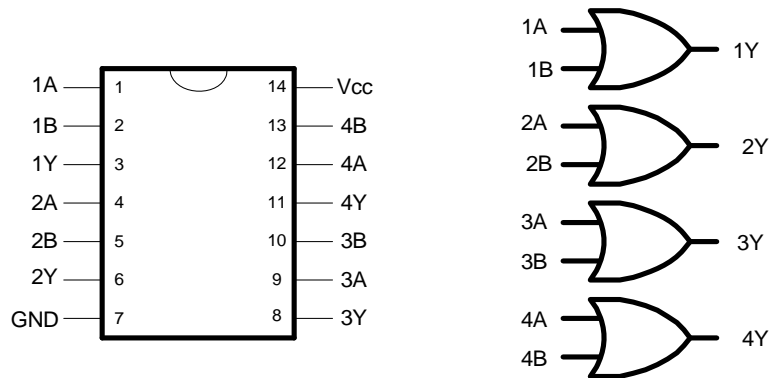


Figure 6.15. The SN7432 Quad 2-input OR gate

Figure 6.16 shows the internal details of the TTL SN7432 Quad 2-input OR gate. We will not describe the functioning of the SN7432 Quad 2-input OR gate at this time. We will defer the circuit operation until we first describe the NOR gate operation in a subsequent section.

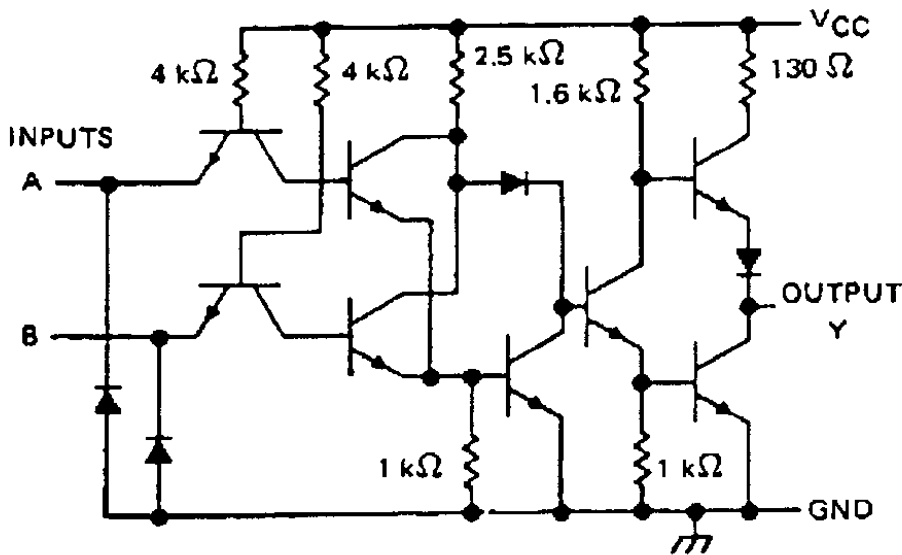


Figure 6.16. Circuit for the SN7432 Quad 2-input OR gate (Courtesy Texas Instruments)

6.6 NAND Gate

The symbol for a 3-input NAND gate is shown in Figure 6.17, and the truth table with positive logic is shown in Table 6.8.

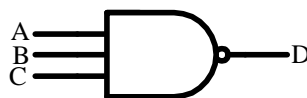


Figure 6.17. Symbol for 3-input NAND gate

TABLE 6.8 Truth table for 3–input NAND gate with positive logic

Inputs			Output
A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 6.8 shows that the output of an NAND gate is logical 0 (false) only when all inputs are logical 1 .

Figure 6.18 shows the TTL SN7400 Quad 2–input NAND gate where Quad implies that there are 4 NAND gates within the IC.

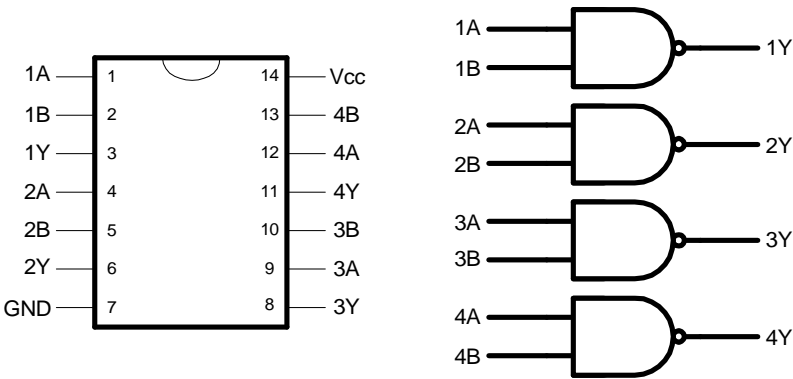
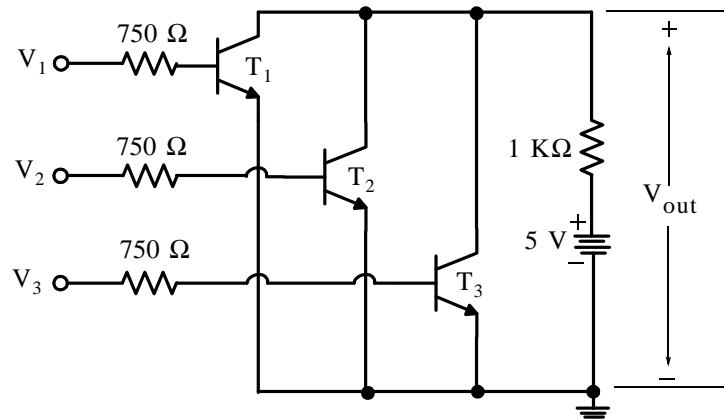


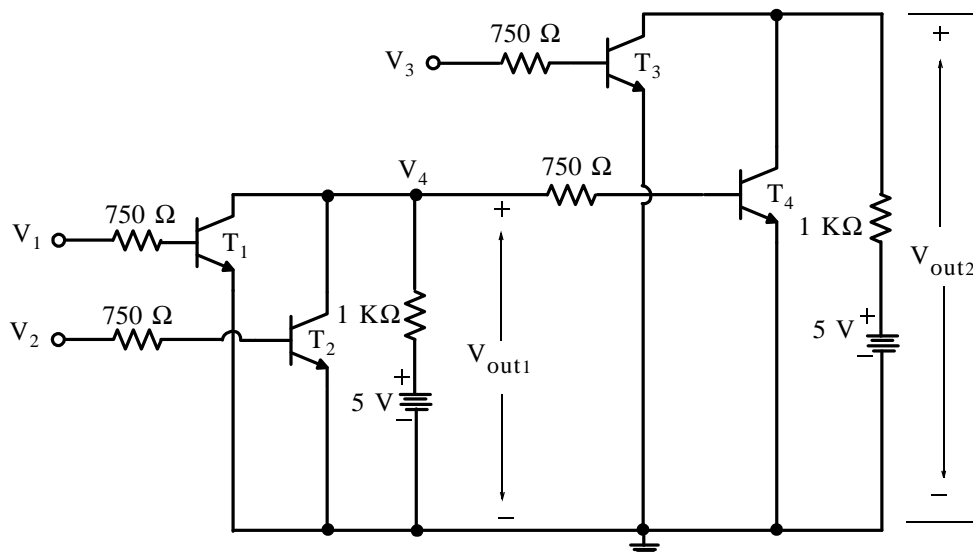
Figure 6.18. The SN7400 Quad 2–input NAND gate

Figure 6.19 shows the internal details of the IC SN7400 NAND gate where transistor T_1 is equivalent to two identical NPN transistors with their bases and collectors tied together; therefore, they are fabricated as a single device with 2 emitters but only one collector and one base as shown in Figure 6.19.



Write the truth table for the input combinations of 0 V and 5 V with respect to the ground. Which type of logic gate does this circuit represent?

5. For the circuit below find V_{out1} and V_{out2} when each of V_1 through V_4 assumes the values of 0 V and 5 V with respect to the ground.



6. For the circuit of Exercise 5, derive an expression for V_{out1} High level when the driving gate has a fan-out of 2. Hint: Start with an equivalent circuit.
7. The circuit below is a 3-input Diode-Transistor Logic (DTL) gate.

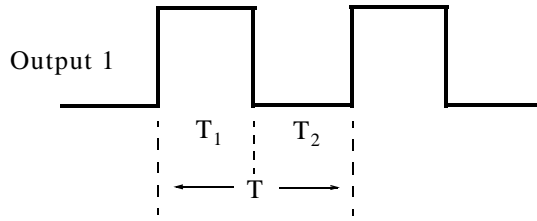


Figure 7.3. Waveform showing period T and times ON and OFF for the multivibrator circuit of Figure 7.1

If in Figure 7.3 $T_1 = T_2$, the pulse repetition frequency f is given by

$$f = \frac{1}{T} = \frac{1}{T_1 + T_2} = \frac{1}{\ln 2 \times R_B \times C} = \frac{1}{0.69 \times R_B \times C}$$

where R_B and C are as shown in Figure 7.1.

7.2 555 Timer

The 555 Timer circuit is a widely used IC for generating waveforms. A simplified diagram is shown in Figure 7.4.

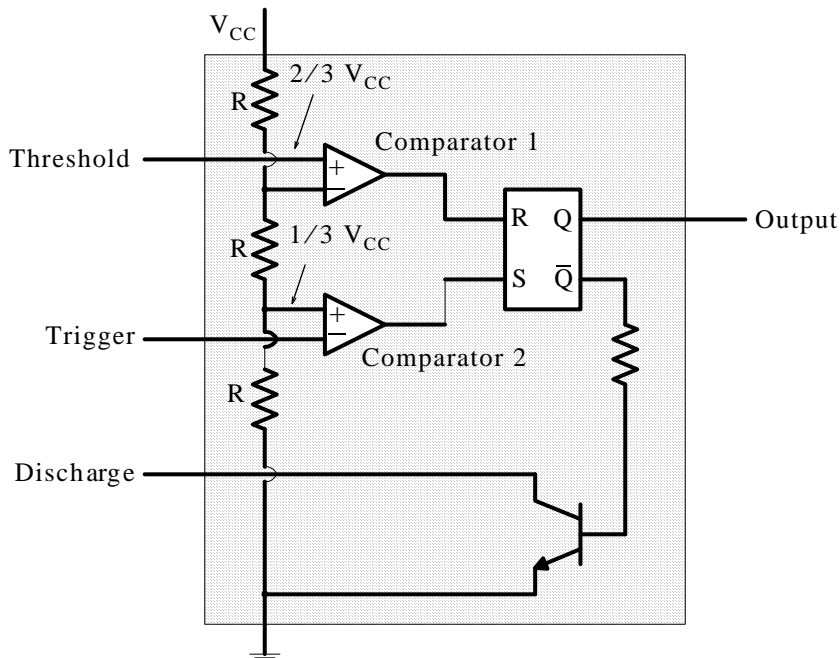


Figure 7.4. Simplified circuit for the 555 Timer

We observe that this IC includes a resistive voltage divider consisting of three identical resistors and this divider sets the voltage at the plus (+) input of the lower comparator at $1/3 V_{CC}$ and at plus (+) input of the upper comparator at $2/3 V_{CC}$. The outputs of the comparators determine the state of the SR flip-flop whose output is either Q or \bar{Q} . Thus, if Q is High (Set state), \bar{Q} is Low, and if Q is Low, \bar{Q} will be High (Reset state) or vice versa.

The SR flip-flop is Set when a High level is applied to the S input, and it is Reset when a High level is applied to the R input. Accordingly, the flip-flop is Set or Reset depending on the outputs of the two comparators, and these outputs are determined by the inputs Threshold at the plus (+) input of Comparator 1, and Trigger at the minus (–) input of Comparator 2. The output of the 555 Timer is the Q output of the SR flip-flop and when it is Low, \bar{Q} will be High, and if the input Discharge is High, the transistor will be saturated and it will provide a path to the ground.

7.3 Astable Multivibrator with the 555 Timer

A useful application of the 555 Timer is as an astable multivibrator. From our previous discussion, we recall that the astable multivibrator is a pulse generator producing waveforms such as that shown in Figure 7.5.

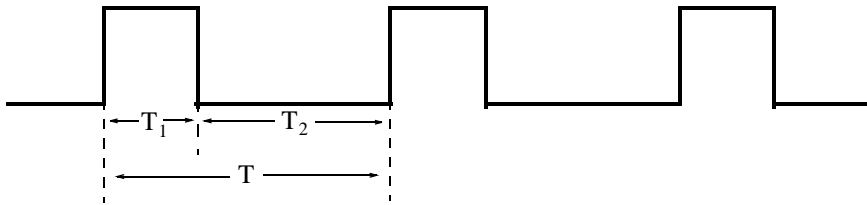


Figure 7.5. Typical waveform for an astable multivibrator

For the waveform of Figure 7.5,

$$\text{Period} = T = T_1 + T_2$$

$$\text{Pulse Repetition Frequency} = f = \frac{1}{T}$$

$$\text{Duty Cycle} = \frac{T_1}{T}$$

Figure 7.6 shows an astable multivibrator employing a 555 Timer. We will see that with this circuit the duty cycle will always be greater than 0.5 as shown in Figure 7.7.

For the circuit of Figure 7.6 let us first assume that the capacitor is uncharged and the SR flip-flop is Set. In this case the output is High and the transistor does not conduct. The capacitor then will charge towards V_{CC} through the resistors R_A and R_B . When the capacitor reaches the value $v_C = 1/3 V_{CC}$ the output of Comparator 2 goes Low and the SR flip-flop remains Set.

When the capacitor reaches the value $v_C = 2/3 V_{CC}$, the output of Comparator 1 goes High and resets the SR flip-flop and thus the output Q goes Low, \bar{Q} goes High, the transistor becomes saturated, its collector voltage becomes almost zero, and since it appears at the common node of resistors R_A and R_B , the capacitor begins to discharge through resistor R_B and the collector of the transistor. The capacitor voltage v_C decreases exponentially with time constant $t_d = R_B C$ and when it reaches the value $v_C = 1/3 V_{CC}$, the output of Comparator 2 goes High and Sets the SR flip-flop.

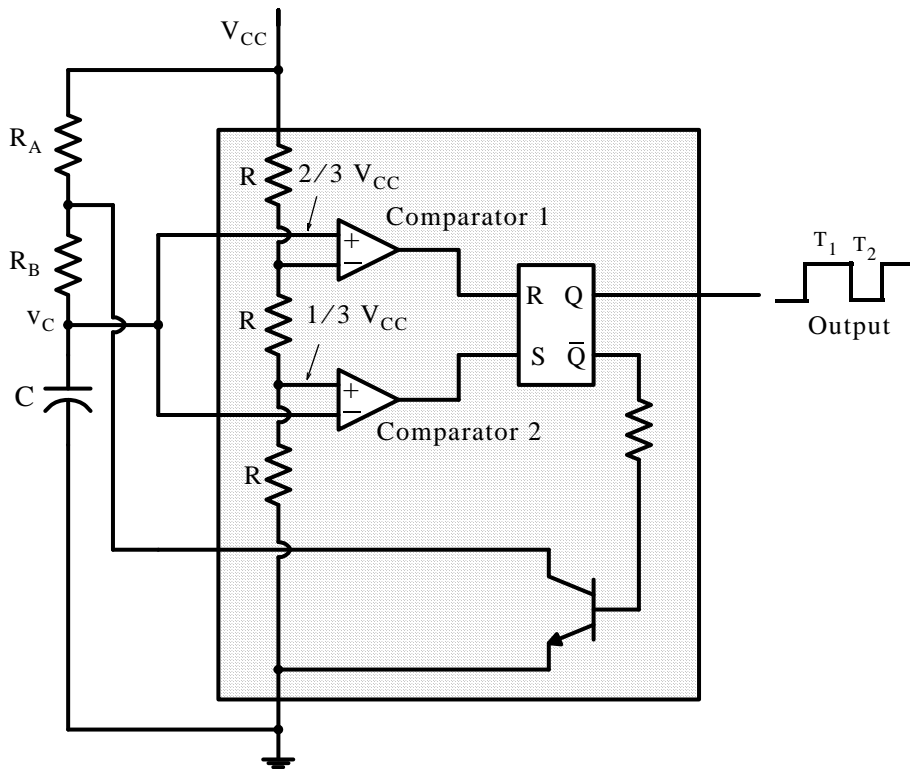


Figure 7.6. Implementation of an astable multivibrator with a 555 Timer

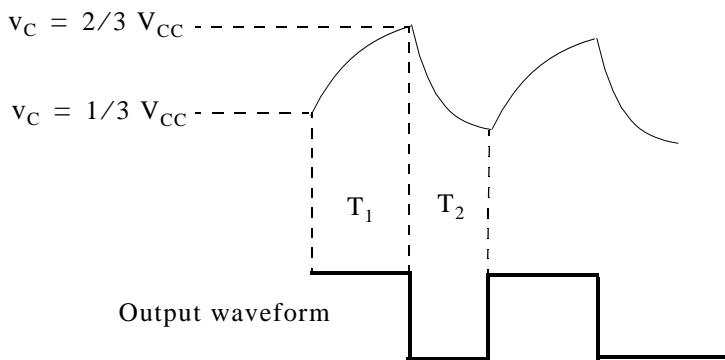


Figure 7.7. Input and output waveforms for the astable multivibrator of Figure 7.6

The output Q goes High, \bar{Q} goes Low, the transistor is turned OFF, the capacitor begins to charge through the series combination of resistors R_A and R_B , and its voltage rises exponentially with time constant $t_r = (R_A + R_B)C$ and when it reaches the value $v_C = 2/3 V_{CC}$ it resets the flip-flop and the cycle is repeated.

We are interested in the pulse repetition frequency $f = 1/T$ and the duty cycle T_1/T where $T = T_1 + T_2$ and the desired values are dependent on appropriate values of resistors R_A and R_B and the capacitor C . As we know, the capacitor voltage as a function of time is given by

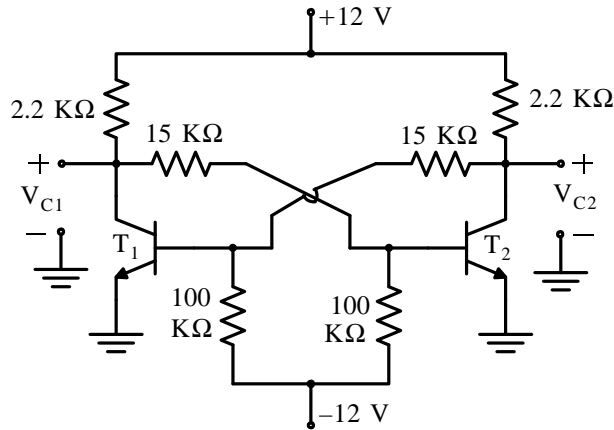


Figure 7.26. Fixed-bias flip-flop circuit for Example 7.4.

Solution:

This circuit consists of two cross-coupled inverter circuits such as that of Exercise 8 in Chapter 6. The analysis is facilitated by breaking the given circuit into two parts, the first part indicating the connections between the base of transistor T_1 and the collector of transistor T_2 as shown in Figure 7.27(a), and the second part indicating the connection between the collector of T_1 and the base of T_2 as shown in Figure 7.27(b).

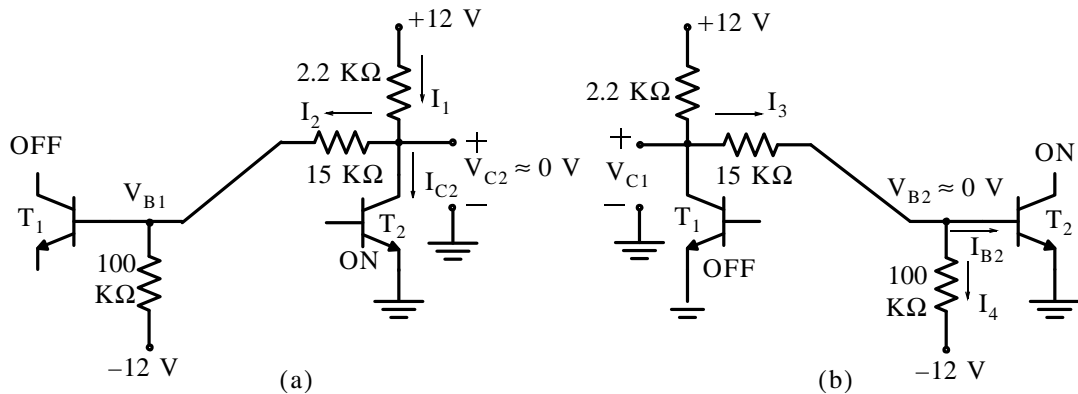


Figure 7.27. Circuits for the computation of the stable states for Example 7.4

Let us first assume that transistor T_1 is OFF and transistor T_2 is ON. Since the saturation voltages are small (about 0.2 V), we will initially neglect them and we let $V_{C2}(\text{sat}) \approx 0 \text{ V}$ and $V_{B2}(\text{sat}) \approx 0 \text{ V}$ as shown in Figures 7.25(a) and 7.25(b) respectively.

By the voltage division expression

$$V_{B1} = \frac{15 \text{ K}\Omega}{100 \text{ K}\Omega + 15 \text{ K}\Omega} \cdot (-12 \text{ V}) = -1.57 \text{ V}$$

and this voltage will certainly keep transistor T_1 at cutoff. To verify that with transistor T_1 beyond cutoff transistor T_2 is in saturation, we calculate I_{C2} by first finding I_1 and I_2 as follows:

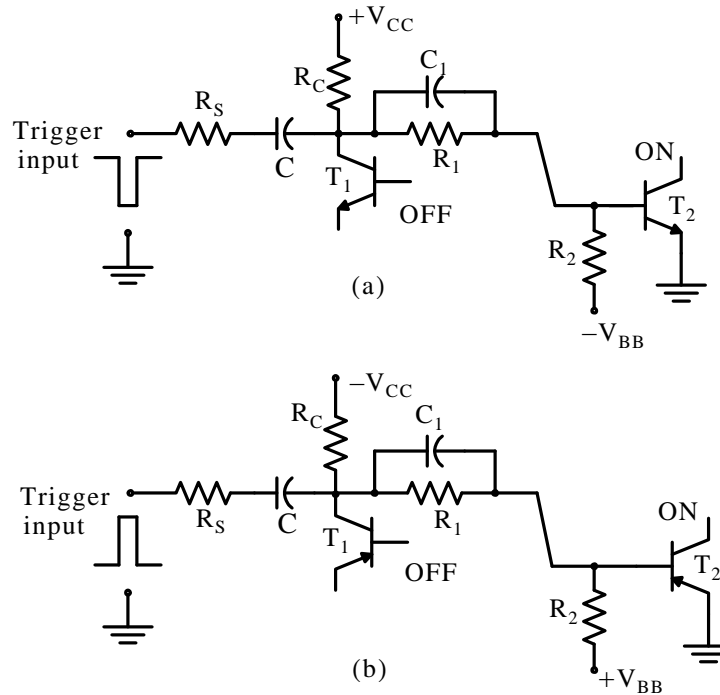


Figure 7.37. A method of triggering unsymmetrically an NPN or a PNP transistor

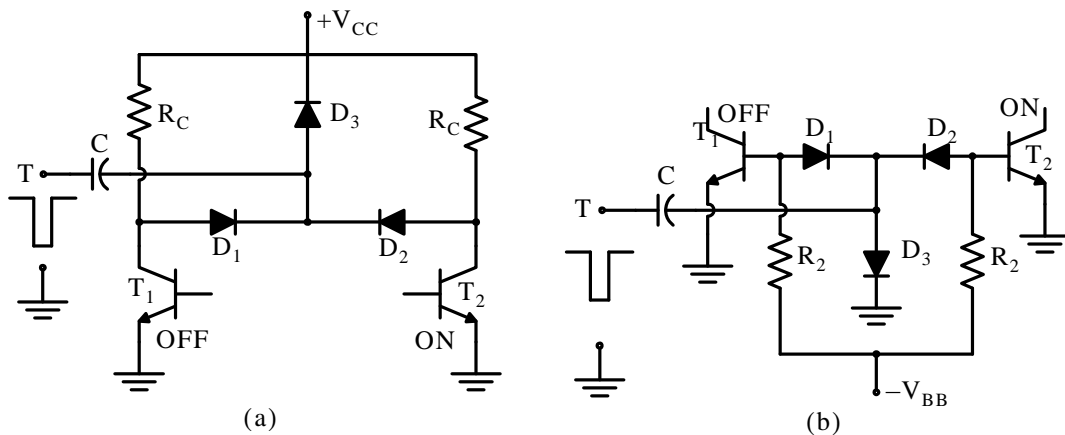


Figure 7.38. Methods of symmetrical triggering through diodes at the collectors or the bases of the transistors

7.5.4 Present Technology Bistable Multivibrators

The bistable multivibrator (flip-flop) circuits we've discussed thus far are the original circuits and were in use in the 1960s. We have included them in this text because they are the circuits from which present technology bistable multivibrators such as those with CMOS technology and op amps have evolved. We will briefly discuss a bistable multivibrator with an op amp in this subsection.

The circuit of Figure 7.39 shows how an op amp can be configured to behave as a bistable multivibrator.

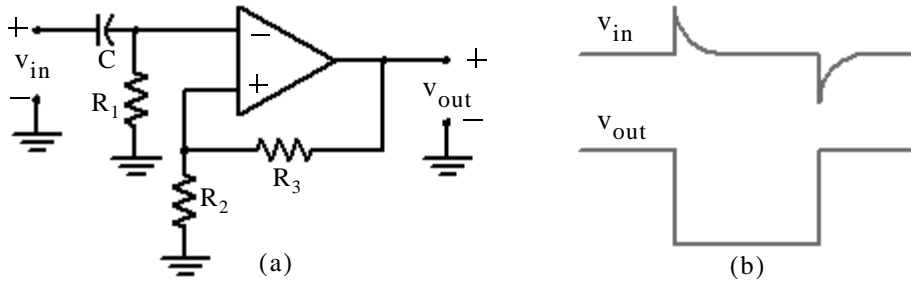


Figure 7.39. Op amp configured as a bistable multivibrator

The stable states for the bistable multivibrator of Figure 7.39(a) are the conditions where the output is at positive or negative saturation. It assumes either positive or negative saturation by the positive feedback formed by resistors R_2 and R_3 . A positive or negative going pulse as that shown in Figure 7.39(b) causes the circuit to switch states.

7.6 Schmitt Trigger

Another bistable multivibrator circuit is the *Schmitt trigger* shown in Figure 7.40(a).

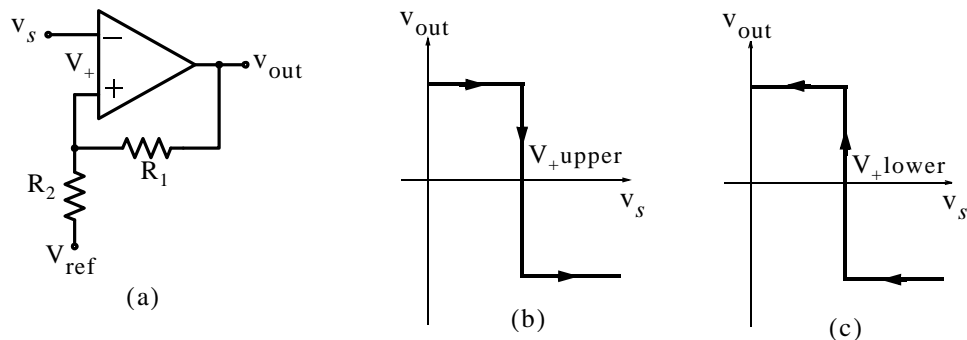
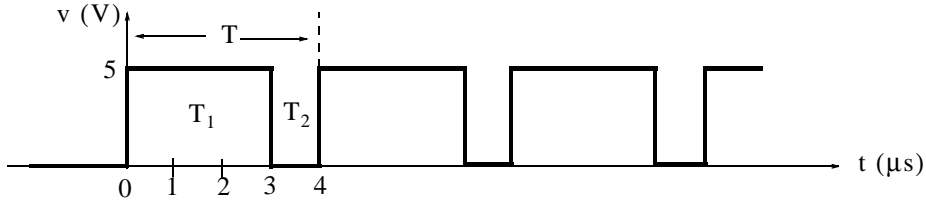


Figure 7.40. Schmitt trigger circuit and waveforms for increasing and decreasing input signals

The *Schmitt trigger* circuit and transfer characteristics are similar to the comparator. It provides an output when its input signal v_s reaches some predetermined value set at the non-inverting input of the op amp. The output of the op amp changes from the positive saturation voltage $V_{out(max)}$ to its negative saturation voltage $-V_{out(max)}$ and vice versa. As shown in Figure 7.40(b), the output is positively saturated as long as the input signal v_s is less than the upper threshold V_{+upper} . If the input signal v_s rises slightly above this threshold voltage, the output drops abruptly to $-V_{out(max)}$ and stays there until v_s drops below a lower threshold voltage V_{+lower} . The threshold voltages V_{+upper} and V_{+lower} are determined by the resistors R_1 and R_2 , and the reference voltage V_{ref} . These threshold voltages can be found by application of KCL at the non-inverting input of the op amp. Thus,

7.9 Solutions to End-of-Chapter Exercises

1.



The period is $T = T_1 + T_2 = 3 + 1 = 4 \mu\text{s}$ and the duty cycle is

$$T_1/T = 3/4 = 0.75 = 75 \%$$

From relation (7.6)

$$T = 4 \times 10^{-6} = 0.69(R_A + 2R_B)C = 0.69 \times 10^{-9}(R_A + 2R_B)$$

$$R_A + 2R_B = \frac{4 \times 10^{-6}}{0.69 \times 10^{-9}} = 5.77 \text{ K}\Omega \quad (1)$$

The duty cycle is T_1/T and from relations (7.3) and (7.6) we obtain

$$\text{Duty cycle} = 0.75 = \frac{T_1}{T} = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} = \frac{R_A + R_B}{R_A + 2R_B} = \frac{R_A + R_B}{5.77 \text{ K}\Omega}$$

$$R_A + R_B = 0.75 \times 5.77 = 4.33 \text{ K}\Omega \quad (2)$$

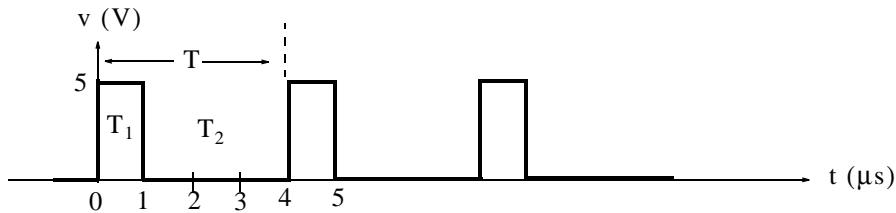
Subtraction of (2) from (1) yields

$$R_B = 5.77 - 4.33 = 3.44 \text{ K}\Omega$$

and from (2)

$$R_A = 4.33 - 3.44 = 890 \Omega$$

2.



The period is $T = T_1 + T_2 = 1 + 3 = 4 \mu\text{s}$. The duty cycle is $T_1/T = 1/4 = 0.25 = 25 \%$. To achieve a duty cycle at 25 %, we must make $T_2 = 3T_1$ and this condition will be satisfied if we multiply relation (7.11) by 3 and equate it to relation (7.14) subject to the constraint of (7.16). Then,

Chapter 8

Frequency Characteristics of Single-Stage and Cascaded Amplifiers

This chapter presents certain basic concepts and procedures that are applicable to frequency dependent single-stage and cascaded amplifiers. The intent is to provide the basic principles of the frequency dependence that is an essential prerequisite for the effective design and utilization of most electronic circuits.

8.1 Properties of Signal Waveforms

In the study of electronic systems we encounter an extremely wide variety of signal waveforms. The simplest are sinusoidal with frequencies of 60 Hz or 400 Hz but in most cases we are concerned with a more complicated class of periodic but non-sinusoidal waveforms. For these waveforms we attempt to represent the signals as a superposition of sinusoidal components of appropriate amplitudes, frequencies, and phases. Fortunately, very powerful techniques for this purpose are available such as the Fourier series,* Fourier transform, and the Laplace transformation.

Periodic signals can be represented as the superposition of sinusoidal components by a Fourier series of the form

$$v(t) = V + V_1 \cos(\omega t + \theta_1) + V_2 \cos(2\omega t + \theta_2) + V_3 \cos(3\omega t + \theta_3) + \dots \quad (8.1)$$

where V is the DC component of the composite signal, ω is the *fundamental frequency* or *first harmonic*, 2ω , is the *second harmonic*, 3ω is the *third harmonic*, and so on.

Unfortunately, not all signals consist of harmonically related components. In the case of speech or music, for instance, the sinusoidal composition of the sound is continuously changing. In this case, the composite signal can be approximated by the superposition of a number of sinusoidal components expressed as

$$v(t) = V + V_1 \cos(\omega_1 t + \theta_1) + V_2 \cos(\omega_2 t + \theta_2) + V_3 \cos(\omega_3 t + \theta_3) + \dots \quad (8.2)$$

where V is the DC component of the composite signal, and ω_1 , ω_2 , ω_3 , and so on, are not harmonically related.

Figure 8.1, referred to as the *frequency spectrum* of the signal reveals information about the frequencies and amplitude, but it contains no information about the phase angles of the components.

* For a thorough discussion on Fourier series, the Fourier transform, and the Laplace transformation please refer to *Signals and Systems with MATLAB Computing and Simulink Modeling*, ISBN 978-1-934404-23-2.

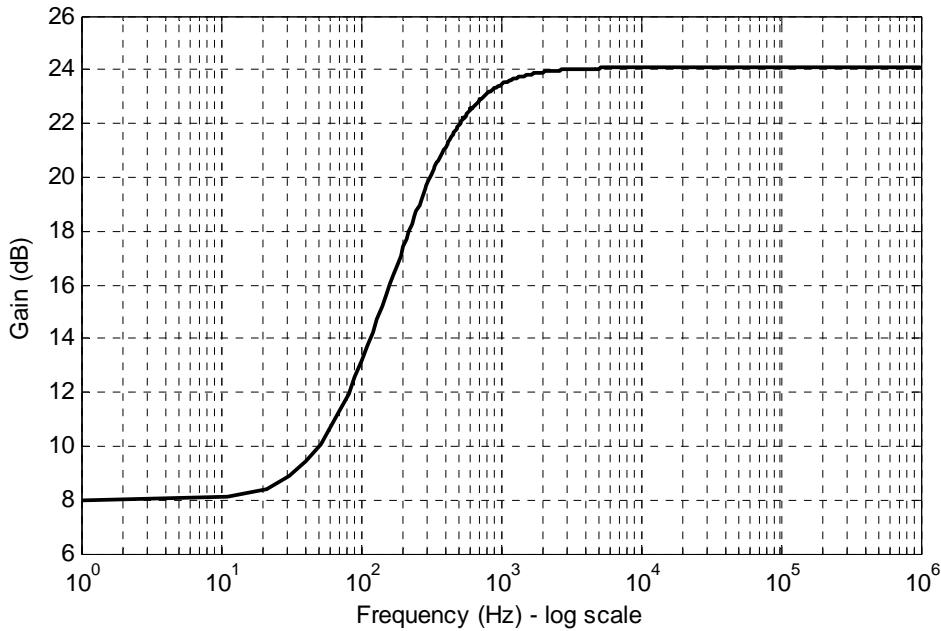


Figure 8.7. Gain versus frequency plot for Example 8.3 with MATLAB

8.3 Transistor Amplifier at High Frequencies

In Chapter 3, Section 3.13, we introduced the hybrid- π model for a transistor at high frequencies and this model is repeated in Figure 8.8 for convenience.

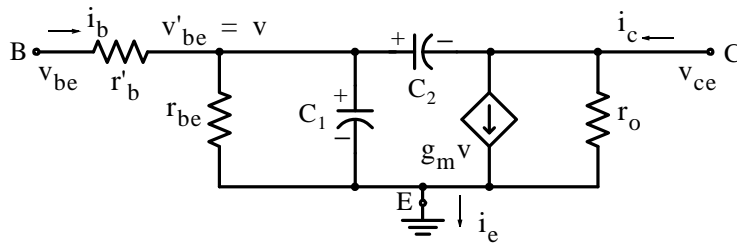


Figure 8.8. The hybrid- π model for the transistor at high frequencies

An incremental model for the transistor amplifier in Figure 8.9(a) that is valid at medium and high frequencies is shown in Fig. 8.9(b).

The transistor circuit of Figure 8.9(a) is represented by the hybrid- π model of Figure 8.9(b), where the resistance R_1 represents resistances R_A , R_B , and the resistance associated with the source I_1 . The behavior of this amplifier is affected at high frequencies by the parasitic capacitances C_e and C_c . At high frequencies, these capacitances tend to short-circuit node b' to ground and this results in a significant reduction of the voltage v and the current $g_m v$.

$k_3 = 47.92$
 $f_3 = 3.27 \text{ Hz}$
 $w_3 = 20.55 \text{ rps}$
 $C_3 = 22.12 \text{ microF}$
 $w_5 = 20.55 \text{ rps}$
 $C_{4d} = 2.92 \text{ microF}$
 $A_m = 87.30$

The plot for the current gain (in dB scale) versus frequency (in log scale) is shown in Figure 8.19.

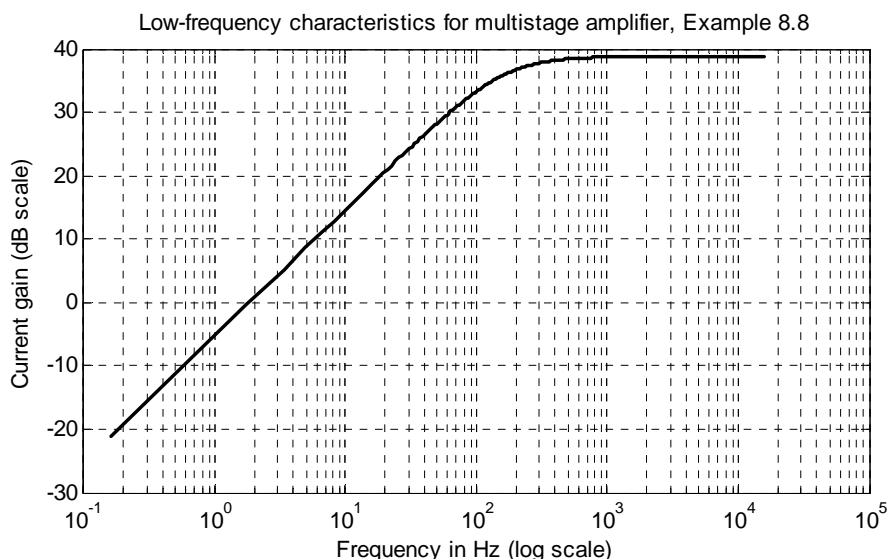


Figure 8.19. Amplitude of current gain versus frequency for Example 8.8

8.6 Overall Characteristics of Multistage Amplifiers

The asymptotes for the amplitude and phase characteristics for a typical RC-coupled stage amplifier are shown in Figure 8.20 where the symbols f_L and f_H define the low- and high-frequency ranges respectively. At low frequencies the voltage gain A_{vL} is obtained from the relation

$$A_{vL} = -A_{mL} \frac{j\omega/\omega_L}{1 + j\omega/\omega_L} \quad (8.63)$$

where A_{mL} depends on the circuit parameters, and ω_L is the low-frequency half-power point. For instance, for the transistor amplifier circuit of Figure 8.5 at low frequencies, $\omega_L = \omega_3$ is as defined in relation (8.11), and A_{mL} is as defined in relation (8.14).

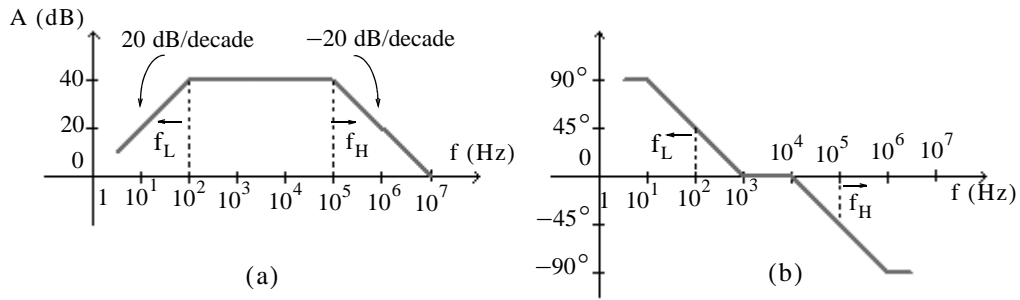


Figure 8.20. Frequency characteristics for a typical single stage amplifier

At high frequencies the voltage gain A_{vH} is obtained from the relation

$$A_{vH} = -A_{mH} \frac{1}{1 + j\omega/\omega_H} \quad (8.64)$$

where A_{mH} depends on the circuit parameters, and ω_H is the high-frequency half-power point. For instance, for the transistor amplifier circuit of Figure 8.9 at high frequencies, $\omega_H = \omega_1$ is as defined in relation (8.28), and A_{mH} is as defined in relation (8.27).

We can obtain the combined low- and high-frequency characteristics for the voltage gain A_v by multiplying relation (8.89) by (8.90); thus,

$$A_v = A_{mL} A_{mH} \frac{j\omega/\omega_L}{(1 + j\omega/\omega_L)(1 + j\omega/\omega_H)} \quad (8.65)$$

If two identical stages such as that shown in Figure 8.18, are connected in cascade, the overall voltage gain A_v is obtained from the relation

$$A_v = A_m^2 \frac{(j\omega/\omega_L)^2}{(1 + j\omega/\omega_L)^2 (1 + j\omega/\omega_H)^2} \quad (8.66)$$

The overall amplitude characteristics for two identical stages in cascade is shown in Figure 8.21.

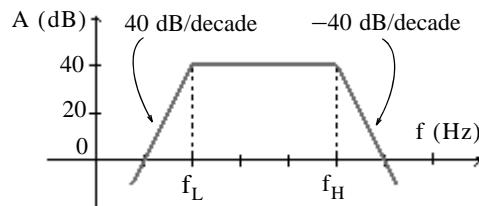


Figure 8.21. Typical overall amplitude characteristics for two identical stages in cascade

By comparing the amplitude characteristics of Figures 8.20 and 8.21, we observe that the bandwidth between the half-power points decreases as more stages are connected in cascade. It can be shown* that the half-power bandwidth of the cascade of n identical stages is given by

* The proof is left as an exercise for the reader at the end of this chapter.

This chapter begins with an introduction to tuned amplifiers. We will examine the properties of various tuned amplifiers that find applications to telecommunications systems employing narrowband modulated signals. New tools for the analysis and design of tuned amplifiers are developed.

9.1 Introduction to Tuned Circuits

The amplifiers discussed in previous chapters are sufficient for most applications in which it is not required that the signals be transmitted over long distances. Thus they are adequate for audio amplifiers used in public address and home entertainment systems, servomechanisms, automatic pilots, electronic instruments, and a host of similar applications. However, when the signals must be transmitted over long distances, as between two cities or between a space vehicle and a ground station, effective use of the transmission medium requires the use of narrowband systems operating at high frequencies. Various systems of this kind operate throughout the frequency spectrum from 10 KHz to about 10 GHz although at the higher end of this range ordinary transistors are not used. For these higher frequencies it is necessary to use tuned amplifiers with RLC coupling to overcome the effects of parasitic capacitances and to provide a filtering operation in the form of frequency-selective amplification. In this section we will introduce the properties of various tuned amplifiers that find application in telecommunication systems.

A *tuned amplifier* is essentially a bandpass filter.* A passive bandpass filter is constructed with passive devices, i.e., resistors, inductors, and capacitors, and thus it provides no gain. For small signals, active filters with op amps are very popular. Tuned amplifiers can also be designed with bipolar junction transistors and MOSFETs, and our subsequent discussion will be based on these devices.

When signals must be transmitted over long distances, either by wire or wireless, efficient utilization of the transmission medium requires the use of high-frequency, narrowband signals. To generate these signals a high-frequency carrier wave, usually a sinusoid, is caused to change instant by instant in accordance with the information signal to be transmitted. The process by which the carrier wave is made to change in accordance with the information signal is called *modulation*. A sinusoid has three characteristics that can be modulated; they are the amplitude, the frequency, and the phase, and they give rise to *amplitude-modulated* (AM), *frequency-modulated* (FM), and *phase-modulated* (PM) signals. To understand the requirements that must be met by tuned amplifiers it is necessary to examine the nature of these waves and to understand the way in which they are used in telecommu-

* For a thorough discussion on passive and active filters, please refer to *Signals and Systems with MATLAB Applications*, ISBN 978-1-934404-23-2.

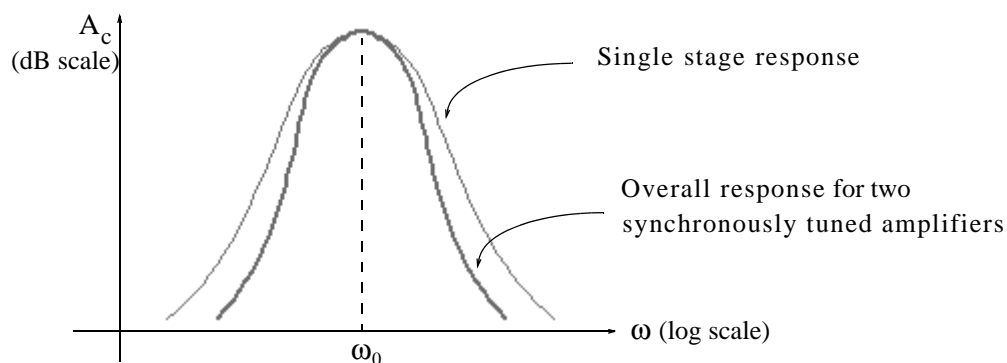


Figure 9.11. Frequency responses for single stage and two synchronously tuned amplifiers.

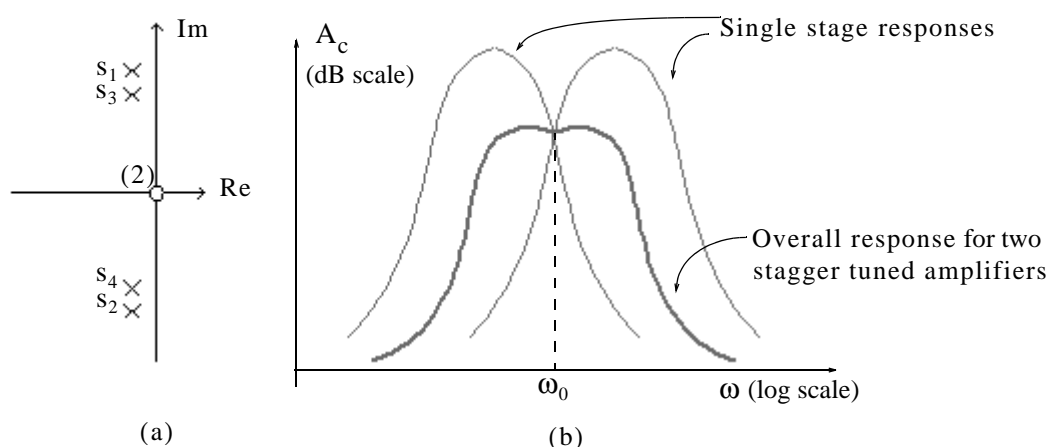


Figure 9.12. Pole-zero pattern and amplitude characteristic for two stagger-tuned amplifiers

Poles s_1 and s_2 in Figure 9.12(a) are the poles one of the stages, and poles s_3 and s_4 are the poles of the other stage; all four poles lie on a line parallel to the imaginary axis. With this arrangement, the amplitude characteristic of the stagger-tuned amplifier will be shown in Figure 9.12(b). We observe that the passband of such stagger-tuned amplifier is wider and flatter than the passband of the synchronously tuned amplifier.

The top flatness of the characteristic depends on the spacing between the poles in Figure 9.12(a), and it is under the control of the designer. Consider, for example the relations (9.20) and (9.21) which are repeated below for convenience, and the pole-zero pattern of Figure 9.10(a).

$$\omega_0^2 = \frac{1}{LC} \quad (9.61)$$

$$2\alpha = \frac{1}{RC} \quad (9.62)$$

From relation (9.62) we observe that if R and C remain constant, the spacing α from the imaginary axis remains constant also. From relation (9.61) we observe that a change in L will result in a change in ω_0 but since α remains constant, the poles must move on a path parallel to the imagi-

nary axis. Hence, the staggering of the poles along the vertical line can be adjusted by adjusting the inductances in the two stages for slightly different values.

We found that the current gain of one stage under sinusoidal conditions and after the narrowband approximations have been applied, is given by relation (9.48), that is,

$$A(j\omega) = -\frac{g_m}{2C} \cdot \frac{1}{j\omega - s_1} \quad (9.63)$$

Therefore, the current gain of a two stagger-tuned amplifier is

$$A(j\omega) = \frac{g_m^2}{4C_1C_2} \cdot \frac{1}{(j\omega - s_1)(j\omega - s_3)} \quad (9.64)$$

where $s_1 = -\alpha + j\beta_1$, $s_3 = -\alpha + j\beta_3$, β is as shown in Figure 9.10(a), C_1 and C_2 are the capacitances of the first and second stages respectively, and the narrowband approximations have reduced a fourth-degree polynomial in the denominator to a second-degree polynomial.

The narrowband approximations and relation (9.64) reveal that the frequency characteristics of the amplifier in the passband are determined by the two poles s_1 and s_3 , and the poles s_2 and s_4 together with the zeros at the origin contribute the constant $1/4$ in the scale factor of that relation. Figure 9.13(a) shows an enlarged view of the pole-zero pattern in the vicinity of the poles s_1 and s_3 .

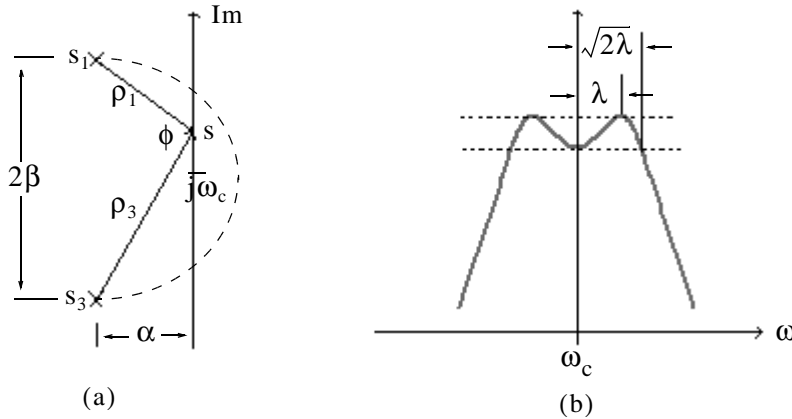


Figure 9.13. Frequency characteristic for two stagger-tuned stages

The frequency ω_c , which is the center frequency of the passband, corresponds to a point on the imaginary axis equidistant from s_1 and s_3 , and the vectors ρ_1 and ρ_3 correspond to the linear factors $j\omega - s_1$ and $j\omega - s_3$. The amplification, given by (9.64), can be expressed as

$$A = \frac{g_m^2}{4C_1C_2} \cdot \frac{1}{\rho_1\rho_3} \quad (9.65)$$

As the variable $s = j\omega$ moves along the imaginary axis, the area of the triangle $s_1 s s_3$ remains con-

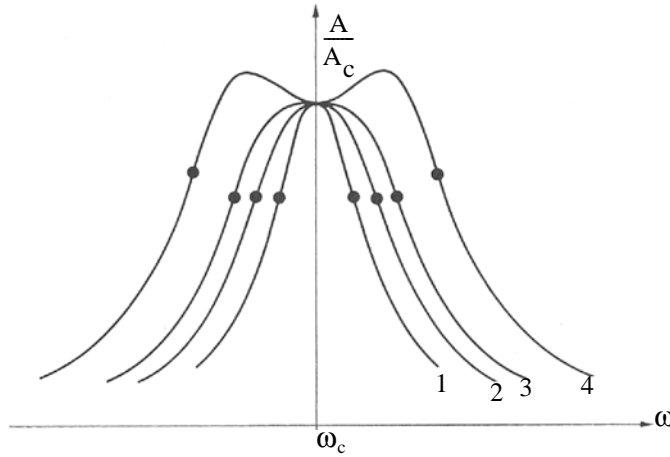


Figure 9.15. Amplitude characteristics for two tuned stages with different degrees of staggering

For the curves in Figure 9.15, α is held constant while β is increased in steps. Curve 1 is for synchronous tuning, Curve 2 is for understaggering with $\phi_c = 70^\circ$, Curve 3 is for flat staggering, and Curve 4 is for overstaggering with $A_p/A_c = 1.1$. The half-power bandwidths are indicated by the solid dots on these curves.

For the flat-staggered case $\beta = \alpha$, $r = 1$, and $\sin\phi_c = 1$. Thus, from relations (9.71) and (9.72) we obtain

$$A_c = A_p = \frac{1}{2}g_m^2 R_1 R_2 \quad (9.85)$$

Letting B_{fs} denote the bandwidth of two stages with flat staggering and BW the 3-dB bandwidth of one of the stages, from (9.84) we obtain

$$B_{fs} = 2\sqrt{2}BW \quad (9.86)$$

The gain-bandwidth product for the flat-staggered amplifier is given by

$$A_c B_{fs} = (1/\sqrt{2})(g_m^2 R_1 R_2)BW \quad (9.87)$$

For two synchronously tuned stages we denote the bandwidth of two stages as B_{syn} . Then, for the gain-bandwidth product, using relation (9.60) we obtain

$$A_c B_{syn} = A_1^2 BW_1 \sqrt{2^{1/2} - 1} = 0.64(g_m^2 R_1 R_2)(BW) \quad (9.88)$$

The foregoing discussion of stagger-tuned amplifiers considers only the case in which the poles are staggered along a line parallel to the imaginary axis. If the poles do not lie on the same vertical line, skewed frequency characteristics result, and, in accordance with the discussion in Section 9.1, this fact may cause distortion of the envelopes of AM signals.

power supply voltage V_{CC} supplied to the transistor is through a path parallel to the tank circuit. In either of the oscillator circuits of Figure 10.5, power through V_{CC} is supplied to the transistor and the tank circuit begins to oscillate. The transistor is operating as Class C amplifier, that is, the transistor conducts for a short period of time and returns sufficient energy to the tank circuit to ensure a constant amplitude output signal. As we've learned in Chapter 3, Class C operation provides the highest efficiency among all amplifier operations.

10.6 Hartley Oscillator

Figure 10.6 shows a simplified version of the *Hartley oscillator*.

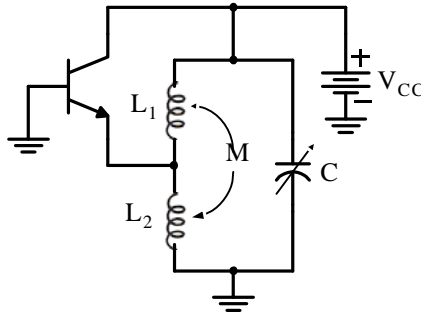


Figure 10.6. Simplified circuit for the Hartley oscillator

In a Hartley oscillator the feedback is provided through a coil pair as shown in Figure 10.4(b). For the oscillator circuit of Figure 10.6 the frequency of oscillation is

$$\omega_0 = \frac{1}{\sqrt{C(L_1 + L_2 + 2M) - (L_1 L_2 - M^2)(h_{ob}/h_{ib})}} \quad (10.14)$$

where M is the *mutual inductance*^{*} and h_{ob} and h_{ib} are the h-parameters representing the output admittance with open-circuit input and input impedance with short circuit output respectively, as discussed in Chapter 3.

10.7 Colpitts Oscillator

Figure 10.7 shows a simplified version of the *Colpitts oscillator*. In a Colpitts oscillator the feedback is provided through a capacitor pair as shown in Figure 10.4(c).

* For a detailed discussion on mutual inductance, please refer to *Circuit Analysis II with MATLAB Computing and Simulink/SimPowerSystems Modeling*, ISBN 978-1-934404-19-5.

$$C_1 \gg C_2.$$

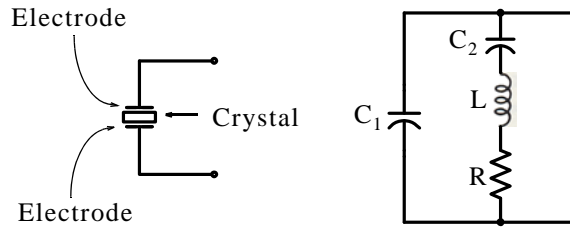


Figure 10.8. Symbol and equivalent circuit for a crystal

The impedance of the equivalent circuit of Figure 10.8 in the s – domain is

$$Z(s) = 1/sC_1 \parallel (R + sL + 1/sC_2) \quad (10.16)$$

We now recall that in a series resonant circuit the quality factor Q at resonance is

$$Q_{0s} = \frac{\omega_{0s}L}{R} \quad (10.17)$$

and since the Q of a crystal oscillator is very high, the value of the resistance R in (10.17) must be very low and thus it can be omitted in relation (10.16) which can now be expressed as

$$Z(s) = 1/sC_1 \parallel (sL + 1/sC_2) = (1/sC_1) \cdot \frac{(sL + 1/sC_2)}{1/sC_1 + sL + 1/sC_2}$$

or

$$Z(s) = (1/sC_1) \cdot \frac{s^2 + 1/LC_2}{s^2 + [(C_1 + C_2)/(LC_1C_2)]} \quad (10.18)$$

The denominator of (10.18) is a quadratic and it implies the presence of two resonant frequencies which can be found by inspection of the equivalent circuit of Figure 10.10. The resonance of the series branch occurs when the imaginary part of the impedance is equal to zero. Thus, letting $s = j\omega$ we obtain $Z(j\omega) = j\omega L + 1/j\omega C_2 = 0$ and denoting this frequency as ω_{0s} we obtain

$$\omega_{0s} = \frac{1}{\sqrt{LC_2}} \quad (10.19)$$

We also can prove* that the resonance of the parallel combination occurs when

$$\omega_{0P} = \sqrt{\frac{C_1 + C_2}{LC_1C_2}} \quad (10.20)$$

As stated above, $C_1 \gg C_2$ and under this condition relation (10.20) reduces to that of relation (10.19).

* The proof is left as an exercise for the reader at the end of this chapter.

This appendix serves as an introduction to the basic MATLAB commands and functions, procedures for naming and saving the user generated files, comment lines, access to MATLAB's Editor / Debugger, finding the roots of a polynomial, and making plots. Several examples are provided with detailed explanations.

A.1 MATLAB® and Simulink®

MATLAB and Simulink are products of The MathWorks,™ Inc. These are two outstanding software packages for scientific and engineering computations and are used in educational institutions and in industries including automotive, aerospace, electronics, telecommunications, and environmental applications. MATLAB enables us to solve many advanced numerical problems rapidly and efficiently.

A.2 Command Window

To distinguish the screen displays from the user commands, important terms, and MATLAB functions, we will use the following conventions:

Click: Click the left button of the mouse

Courier Font: Screen displays

Helvetica Font: User inputs at MATLAB's command window prompt `>>` or `EDU>>` *

Helvetica Bold: MATLAB functions

Normal Font Bold Italic: Important terms and facts, notes and file names

When we first start MATLAB, we see various help topics and other information. Initially, we are interested in the *command screen* which can be selected from the Window drop menu. When the command screen, we see the prompt `>>` or `EDU>>`. This prompt is displayed also after execution of a command; MATLAB now waits for a new command from the user. It is highly recommended that we use the *Editor/Debugger* to write our program, save it, and return to the command screen to execute the program as explained below.

To use the Editor/Debugger:

1. From the *File* menu on the toolbar, we choose *New* and click on *M-File*. This takes us to the *Editor Window* where we can type our *script* (list of statements) for a new file, or open a previously saved file. We must save our program with a file name which starts with a letter. ***Important!*** MATLAB is *case sensitive*, that is, it distinguishes between upper- and lower-case letters. Thus, *t*

* `EDU>>` is the MATLAB prompt in the Student Version

This appendix is a brief introduction to Simulink. This author feels that we can best introduce Simulink with a few examples. Some familiarity with MATLAB is essential in understanding Simulink, and for this purpose, Appendix A is included as an introduction to MATLAB.

B.1 Simulink and its Relation to MATLAB

The MATLAB® and Simulink® environments are integrated into one entity, and thus we can analyze, simulate, and revise our models in either environment at any point. We invoke Simulink from within MATLAB. We will introduce Simulink with a few illustrated examples.

Example B.1

For the circuit of Figure B.1, the initial conditions are $i_L(0^-) = 0$, and $v_C(0^-) = 0.5$ V. We will compute $v_C(t)$.

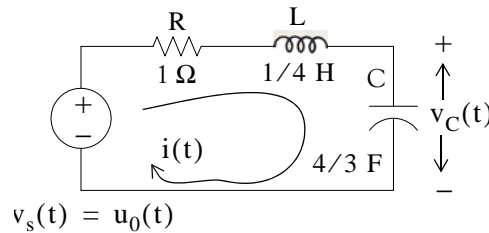


Figure B.1. Circuit for Example B.1

For this example,

$$i = i_L = i_C = C \frac{dv_C}{dt} \quad (\text{B.1})$$

and by Kirchoff's voltage law (KVL),

$$Ri_L + L \frac{di_L}{dt} + v_C = u_0(t) \quad (\text{B.2})$$



Substitution of (B.1) into (B.2) yields

$$RC \frac{dv_C}{dt} + LC \frac{d^2 v_C}{dt^2} + v_C = u_0(t) \quad (\text{B.3})$$

Absolute tolerance: auto

Now, we switch to the MATLAB Command prompt and we type the following:

```
a0=1; a1=0; a2=2; a3=0; x0=[0 0 0 0]';
```

We change the **Simulation Stop time** to 25, and we start the simulation by clicking on the  icon. To see the output waveform, we double click on the **Scope** block, then clicking on the Autoscale  icon, we obtain the waveform shown in Figure B.17.

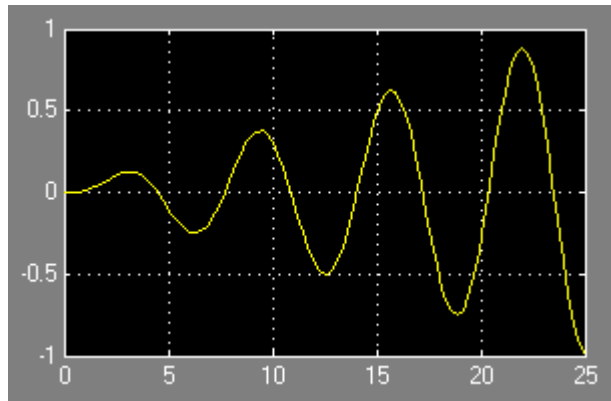


Figure B.17. Waveform for Example B.2

The **Display** block in Figure B.17 shows the value at the end of the simulation stop time.

Examples B.1 and B.2 have clearly illustrated that the **State–Space** is indeed a powerful block. We could have obtained the solution of Example B.2 using four Integrator blocks by this approach would have been more time consuming.

Example B.3

Using **Algebraic Constraint** blocks found in the **Math Operations** library, **Display** blocks found in the **Sinks** library, and **Gain** blocks found in the **Commonly Used Blocks** library, we will create a model that will produce the simultaneous solution of three equations with three unknowns.

The model will display the values for the unknowns z_1 , z_2 , and z_3 in the system of the equations

$$\begin{aligned}a_1 z_1 + a_2 z_2 + a_3 z_3 + k_1 &= 0 \\a_4 z_1 + a_5 z_2 + a_6 z_3 + k_2 &= 0 \\a_7 z_1 + a_8 z_2 + a_9 z_3 + k_3 &= 0\end{aligned}\tag{B.40}$$

The model is shown in Figure B.18.

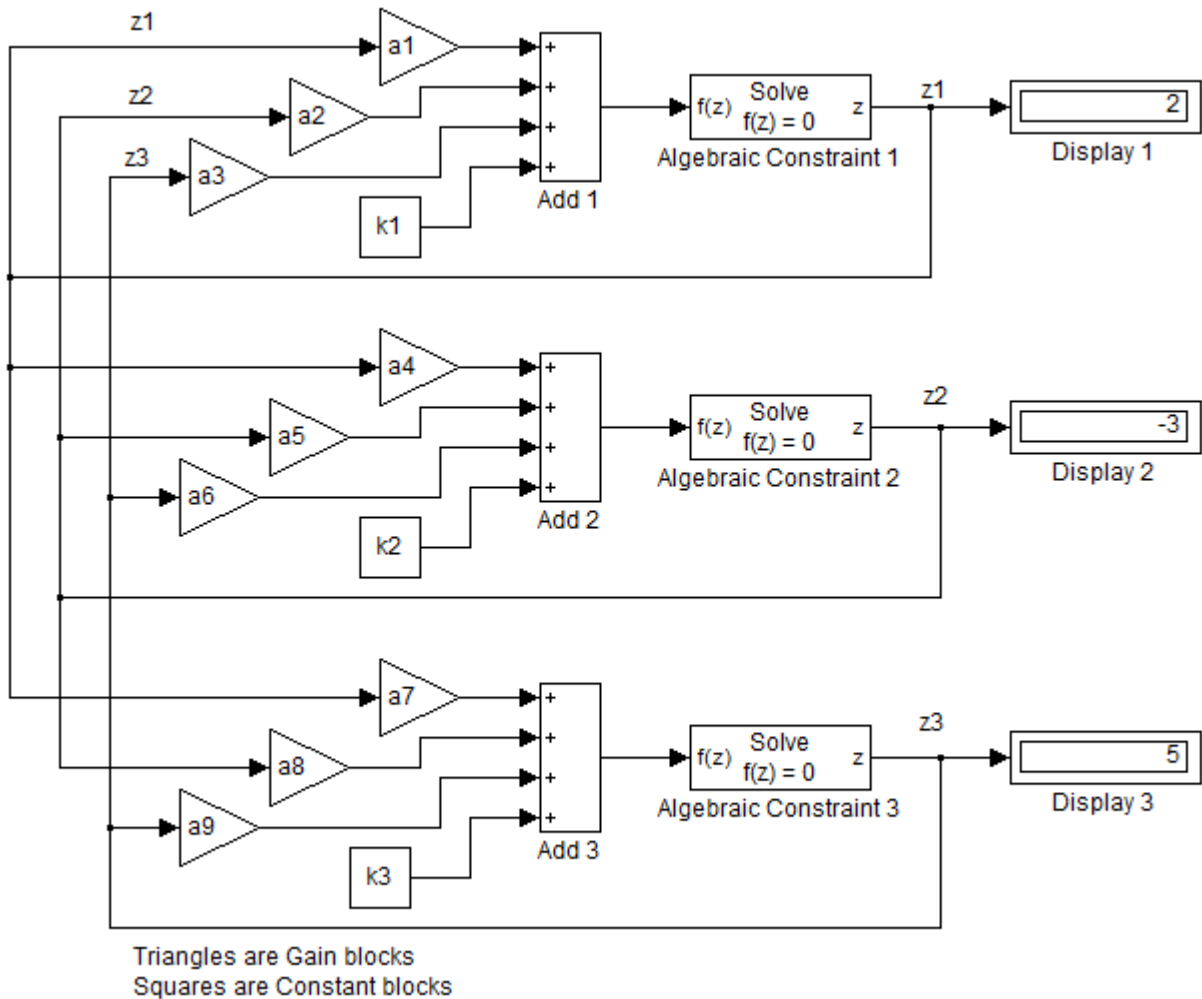


Figure B.18. Model for Example B.3

Next, we go to MATLAB's Command prompt and we enter the following values:

$a_1=2$; $a_2=-3$; $a_3=-1$; $a_4=1$; $a_5=5$; $a_6=4$; $a_7=-6$; $a_8=1$; $a_9=2$; $k_1=-8$; $k_2=-7$; $k_3=5$;

After clicking on the simulation icon, we observe the values of the unknowns as $z_1 = 2$, $z_2 = -3$, and $z_3 = 5$. These values are shown in the **Display** blocks of Figure B.18.

The **Algebraic Constraint** block constrains the input signal $f(z)$ to zero and outputs an algebraic state z . The block outputs the value necessary to produce a zero at the input. The output must affect the input through some feedback path. This enables us to specify algebraic equations for index 1 differential/algebraic systems (DAEs). By default, the Initial guess parameter is zero. We can improve the efficiency of the algebraic loop solver by providing an Initial guess for the algebraic state z that is close to the solution value.

An outstanding feature in Simulink is the representation of a large model consisting of many blocks and lines, to be shown as a single Subsystem block.* For instance, we can group all blocks and lines in the model of Figure B.18 except the display blocks, we choose **Create Subsystem** from the **Edit** menu, and this model will be shown as in Figure B.19† where at the MATLAB command prompt we have entered:

`a1=5; a2=-1; a3=4; a4=11; a5=6; a6=9; a7=-8; a8=4; a9=15; k1=14; k2=-6; k3=9;`

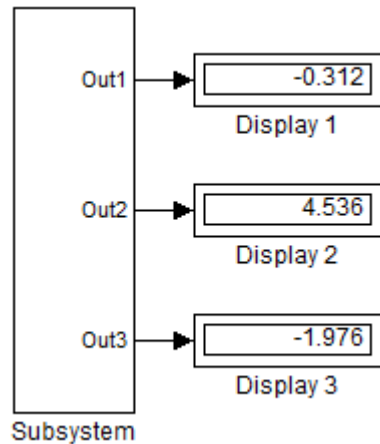


Figure B.19. The model of Figure B.18 represented as a subsystem

The Display blocks in Figure B.19 show the values of z_1 , z_2 , and z_3 for the values specified at the MATLAB command prompt.

B.2 Simulink Demos

At this time, the reader with no prior knowledge of Simulink, should be ready to learn Simulink's additional capabilities. It is highly recommended that the reader becomes familiar with the block libraries found in the Simulink Library Browser. Then, the reader can follow the steps delineated in The MathWorks Simulink User's Manual to run the Demo Models beginning with the **thermo** model. This model can be accessed by typing

thermo

at the MATLAB command prompt.

* The Subsystem block is described in detail in *Introduction to Simulink with Engineering Applications, Third Edition*, ISBN 978-1-934404-21-8, Example C.1, Page C-1, Appendix C

† The contents of the Subsystem block are not lost. We can double-click on the Subsystem block to see its contents. The Subsystem block replaces the inputs and outputs of the model with Inport and Outport blocks. These blocks are also described in *Introduction to Simulink with Engineering Applications, Third Edition*, ISBN 978-1-934404-21-8, Example C.1, Page C-1, Appendix C.

This appendix is a brief introduction to the Simscape and its libraries. Our discussion will be on the **Foundation**, **SimElectronics**, **SimPowerSystems**, and **Utilities** libraries. The Simscape main library also includes the SimDriveline, SimHydraulics, and SimMechanics libraries, and these will not be discussed in this appendix.

C.1 Simscape Libraries

The Simulink models consist of blocks which represent mathematical operations, addition, subtraction, multiplication, division, differentiation, integration, and combinations of these. A Simulink model is thus a mathematical model of a system to be designed. Simscape, on the other hand, is a set of block libraries in a Physical Network that represents a physical system layout with blocks representing physical components with units of measurement. A Simscape model can also be thought of an engineering drawing from which a system can be assembled.

Simscape has its own libraries of blocks and allows us to connect Simulink blocks as sources and sinks such as XY Graphs and Scope blocks. The **Simscape** libraries discussed in this appendix are shown in Figure C.1. It can be accessed by typing **simscape** at the MATLAB command prompt or through the **Simulink Library Browser**. The Simulink documentation refers the **Foundation** and **Utilities** libraries as top-level libraries.

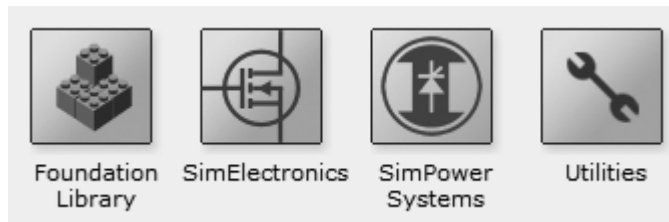


Figure C.1. The Simscape libraries discussed in this appendix

C.1.1 Foundation Library

The Foundation library contains the blocks shown in Figure C.2

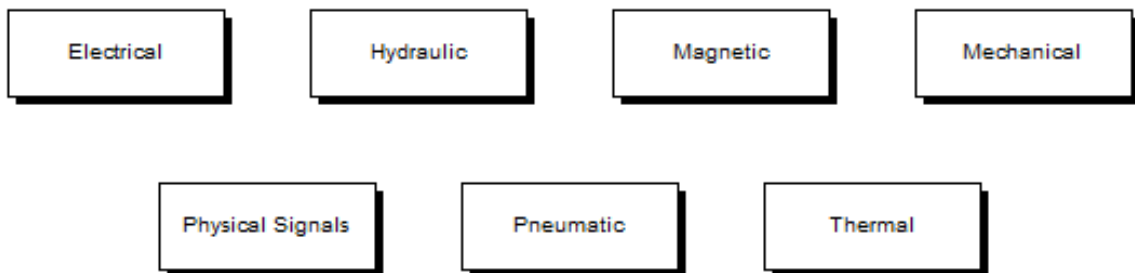


Figure C.2. The contents of the Foundation Library

Appendix D

Proportional–Integral–Derivative (PID) Controller

This appendix is a brief introduction to the Proportional–Integral–Derivative Controller, briefly known as PID. The components and the functions of a typical PID are described, and two examples are presented using the Simulink PID Controller Block and the Simulink PID Controller with Approximate Derivative Block.

D.1 Description and Components of a Typical PID

A **proportional–integral–derivative (PID) controller** is a control loop feedback system used in industrial control systems. A PID controller attempts to correct the error between a measured process variable and a desired setpoint by calculating and then outputting a corrective action that can adjust the process accordingly.

The PID controller calculation contains three separate parameters; the **Proportional**, the **Integral**, and **Derivative** values as shown in Figure D.1.

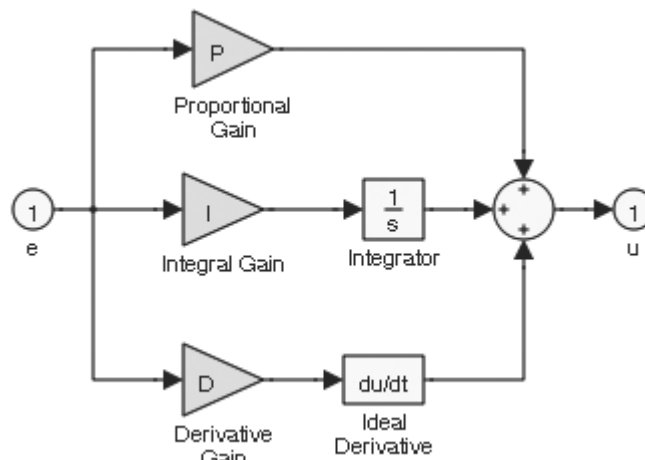


Figure D.1. The components of a typical PID

The Proportional value determines the reaction to the current error, the Integral determines the reaction based on the sum of recent errors, and the Derivative determines the reaction to the rate at which the error has been changing. The weighted sum of these three actions is used to adjust the process via a control element such as the position of a control valve or the power supply of a heating element.

By adjusting the three constants in the PID controller algorithm the PID can provide control action designed for specific process requirements. The response of the controller can be described in terms of the responsiveness of the controller to an error, the degree to which the controller overshoots the setpoint and the degree of system oscillation. The use of the PID algorithm for control does not necessarily result in an optimal configuration for the system.

This appendix begins with a simple resistive attenuator which may be used to reduce the amplitude of a signal waveform. We will examine the conditions under which it is possible to ensure no distortion even if shunt capacitances are taken into consideration. Also, we will investigate the types of responses which are obtained with a step voltage input if the circuit is improperly adjusted.

E.1 Uncompensated Attenuator

Let us consider the simple resistor combination of Figure E.1(a).

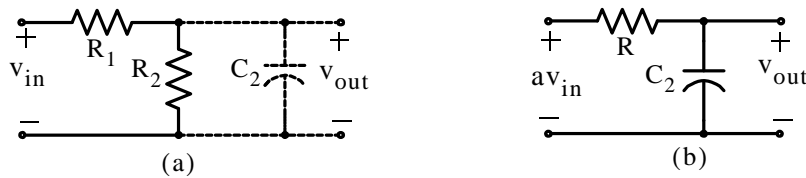


Figure E.1. Actual and equivalent circuit for an uncompensated attenuator

The presence of the stray capacitance C_2 in Figure E.1(a) represents an unavoidable condition since the output of the resistive attenuator in most cases is followed by the input capacitance of a stage of amplification. Using Thevenin's theorem, we can replace the circuit of (a) with that of (b) where R represents the parallel combination of R_1 and R_2 and a in av_{in} is the attenuation factor. We could make both R_1 and R_2 very large so that the input impedance of the attenuator would be large enough to prevent loading down the input signal but this may produce a large rise time which would, in most cases, be unacceptable. This is explained below.

The *rise time*, denoted as t_r , is defined as the time it takes the voltage to rise from 10% to 90% of its final value. It is an indication of how fast a circuit can respond to a discontinuity in voltage. In an RC network the time required for the output voltage v_{out} to reach 10% of its final value is $0.1RC$, and the time required for the output voltage v_{out} to reach 90% of its final value is $2.3RC$. The rise time t_r is the difference between these two values and in terms of the RC time constant τ it is given by

$$t_r = 2.2\tau = 2.2RC = \frac{2.2}{2\pi f_c} = \frac{0.35}{f_c} \quad (E.1)$$

where f_c is the 3-dB frequency given by $f_c = 1/2\pi RC$.

It was stated above that we could make the input impedance of the attenuator large enough to pre-

Appendix F

Substitution, Reduction, and Miller's Theorems

This appendix discusses three additional theorems that are especially useful in the simplification of circuits containing dependent sources. In our previous studies* we discussed the superposition principle and Thevenin's and Norton's theorems.

F.1 Substitution Theorem

The *substitution theorem* states that if the voltage across a branch with nodes x and y of a network is v_{xy} and the current through this branch is i_{xy} , a different branch may be substituted in its place in the network provided that the voltage across the substitute branch is also v_{xy} and the current through it is also i_{xy} . The most common use of this theorem is to replace an impedance by a voltage or current source, or vice versa. The substitution theorem can best be illustrated with the simple circuit and the substitute branches shown in Figure F.1.

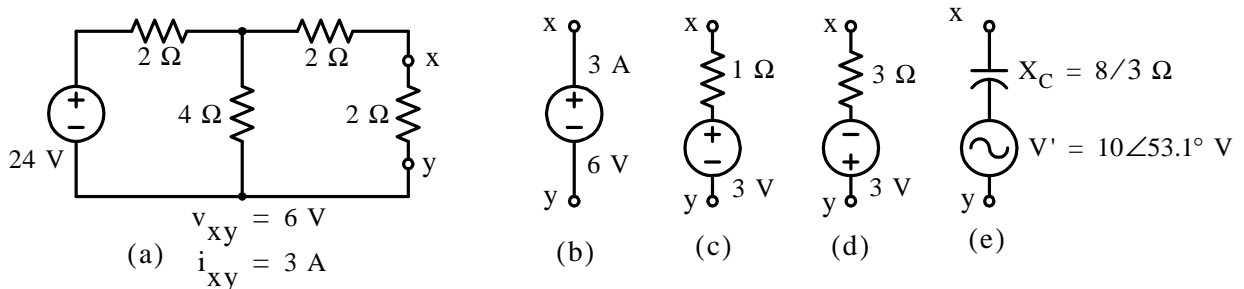


Figure F.1. Illustration of the substitution theorem

For the simple resistor circuit of Figure F.1(a) we find by series–parallel resistance combinations that $v_{xy} = 6\text{ V}$ and $i_{xy} = 3\text{ A}$. According to the substitution theorem, the $2\ \Omega$ resistor across terminals x and y can be replaced with a source with a 6 V source as shown in Figure F.1(b) and the rest of the network will be unaffected. The current in the branch will be 3 A as before.

Other substitutions are possible also. For instance, the substitute branch may consist of a resistance of $1\ \Omega$ and a voltage source of 3 V as shown in Figure F.1(c), or it may consist of a resistance of $3\ \Omega$ and a voltage source of 3 V of opposite polarity as shown in Figure F.1(d).

The voltage source in Figure F.1(a) could be DC or AC. If it is an AC source, we can substitute the $2\ \Omega$ resistor across terminals x and y with a branch that has capacitive reactance in series with a

* For a detailed discussion of Thevenin's and Norton's theorems and the superposition principle please refer to *Circuit Analysis I with MATLAB Applications*, ISBN 978-1-934404-17-9.

F.3 Miller's Theorem

Miller's theorem states that under certain conditions, to be established below, the networks of Figures F.15(a) and F.15(b) are equivalent.

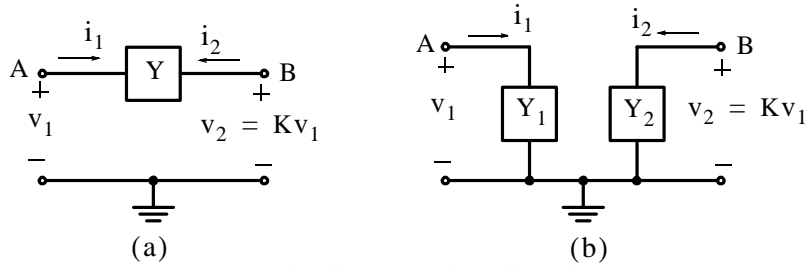


Figure F.15. Illustration for Miller's theorem

In the networks of Figure F.15, the constant K denotes the voltage gain from Node A to Node B, that is,

$$K = v_2/v_1 \quad (F.6)$$

or

$$v_2 = Kv_1 \quad (F.7)$$

At Node A of Figure F.15(a), we observe that

$$i_1 = Y(v_A - v_B) = Y(v_1 - v_2) = Y(v_1 - Kv_1) = Yv_1(1 - K) \quad (F.8)$$

and at Node A of Figure F.15(b), we obtain,

$$i_1 = Y_1 v_1 \quad (F.9)$$

For equivalence, relations (F.8) and (F.9) must be equal. Thus,

$$Y_1 = Y(1 - K) \quad (F.10)$$

At Node B of Figure F.15(a), we observe that

$$i_2 = -i_1 = -Y(v_1 - v_2) = Y(v_2 - v_1) = Y(v_2 - v_2/K) = Yv_2(1 - 1/K) \quad (F.11)$$

and at Node B of Figure F.15(b), we obtain,

$$i_2 = Y_2 v_2 \quad (F.12)$$

For equivalence, relations (F.11) and (F.12) must be equal. Thus,

$$Y_2 = Y(1 - 1/K) \quad (F.13)$$

We should remember that for the equivalent circuit of Figure F.15(b) the value of the gain K , once established, it cannot be changed. Thus, while Miller's theorem can be applied to find the input impedance, it should not be used to determine the output impedance of an amplifier since when

Index

Symbols

% (percent) symbol in MATLAB A-2

Numerics

3 dB point 5-10
3dB point 5-9
555 Timer 7-2

A

A/D conversion 5-55
abs(z) MATLAB function A-22
accuracy 5-61
active filter 5-8
active mode 3-3
active pull-up 6-18
active Region 3-76
ADC (analog- to-digital converter) 5-55
Advanced Low-power Schottky Transistor 6-40
alternating waveform 1-2
amount of feedback 10-2
amplifier defined 1-3
amplitude-modulated signal 9-1
analog-to-digital converter 5-55
analog computers 5-62
AND gate 6-1
angle(z) MATLAB function A-22
anode 2-5
Armstrong oscillator 10-6
astable multivibrator 7-1
attenuation factor 7-12
attenuator 1-3, 5-9
autoscale icon in Simulink B-12
avalanche region 2-7
average value 1-1
averaging op amp 5-37
axis MATLAB command A-15

B

backward diode 2-45
band-elimination filter 5-10
bandpass amplifiers 9-4
band-pass filter 5-10
bandpass filter 9-1
band-rejection filter 5-10
band-stop filter 5-10
bandwidth 1-5
Barkhausen criterion 10-4
barrier 2-5
base spreading resistance 3-44
basic differentiator circuit 5-34
beta cutoff frequency 3-56
BiCMOS 2-input NAND gate 6-41

BiCMOS inverter 6-40
Bistable multivibrator 7-21
bode(sys) MATLAB function 1-12, 1-21
bode(sys,w) MATLAB function 1-13, 1-21
bodemag(sys,w) MATLAB function 1-13, 1-21
bound electrons 2-2
box MATLAB command A-11
buffer 6-17, 6-35
buffer amplifier 5-15
Butterworth configuration 9-26

C

Cascaded Tuned Amplifiers 9-13
cathode. 2-5
cesium oscillators 10-8
Class A Amplifier Operation 3-30
Class AB Amplifier Operation 3-35
Class B Amplifier Operation 3-33
Class C Amplifier Operation 3-37
Class D amplifier 3-37
Class E amplifier 3-37
clc MATLAB command A-2
clear MATLAB command A-2
closed loop transfer function 5-29
closed-loop 5-24
closed-loop gain 5-26
CMOS 4-20
CMOS Logic Gates 6-32
CMOS transmission gate 6-37
CMRR 5-40
collector output resistance 3-10
Colpitts oscillator 10-7
column vector in MATLAB A-17
combinational logic circuit 7-1, 10-1
command screen in MATLAB A-1
command window in MATLAB A-1
comment line in MATLAB A-2
common mode gain 5-40
common mode rejection ratio 5-40
common-base current gain 3-4
common-collector current gain 3-5
common-emitter gain 3-4
comparator 5-24, 5-48, 5-55
compensated attenuator E-2
Complementary Metal Oxide Semiconductor (CMOS) 6-2
Complementary MOS 4-20
complex conjugate A-4
complex numbers A-2
conduction angle 4-26
conv(a,b) MATLAB function A-6
coupling capacitor 8-20
covalent bonding 2-1
Cramer's rule 5-98

critical (cutoff) frequency 5-9
crossover distortion 3-35
crystal oscillators 10-8
current amplifier 1-17
current mirror 4-20
current source absorption F-4
cutoff frequency 1-5, 5-9
cutoff region 3-76, 4-9, 4-23

D

DAC (Digital-to Analog Converter) 5-51, 5-55
DAC with binary-weighted resistors 5-52
DAC with buffered output and gain 5-55
Darlington connection. 3-58
data bus 6-38
data points in MATLAB A-13
data sheets 6-20
dB 1-3
decade 1-7
decibel 1-3, A-12
deconv(p,q) MATLAB function A-7
default color A-14
default line in MATLAB A-14
default marker in MATLAB A-14
default value in MATLAB A-11
degenerative feedback 5-24, 10-2
demo in MATLAB A-2
depletion region 2-4
depletion-mode 4-7
diac 4-24
differential circuit 6-24
differential gain 5-40
differential input 5-1
differential input amplifier 5-1
differential input integrator 5-78
differential input op amp 5-38
differentiator 5-34
digital-to-analog converter 5-51, 5-55
diode detector 2-36, 9-2
Display blocks in Simulink B-18
display formats in MATLAB A-29
doping 2-3
dot multiplication operator in MATLAB A-19
drain 4-1
driver gate 6-18
dual-slope ADC 5-59

E

Early Voltage 3-10
Ebers-Moll Transistor Model 3-79
ECL 6-24
ECL circuit 6-26

editor window in MATLAB A-1
 editor/debugger A-1, A-2
 effect of temperature 3-9
 effective (or RMS) value 1-2
 electromagnetic interference 4-26
 element-by-element division
 in MATLAB A-19
 element-by-element exponentiation
 in MATLAB A-19
 element-by-element multiplication
 in MATLAB A-17, A-19
 EMI 4-26
 emitter diffusion resistance 3-44
 emitter-coupled logic
 (ECL) 6-2, 6-24, 6-26
 enhancement-mode 4-7
 envelope detector 2-36, 9-2
eps MATLAB function A-21, A-25
 equivalence gate 6-16
 equivalent circuit of the inverting
 op amp 5-12
 equivalent circuits 3-7
 error detector circuit 4-26
 Exclusive OR gate 6-1
 Exclusive-NOR gate 6-16
exit MATLAB command A-2
expand(s) MATLAB function 1-14
 external frequency
 compensation 5-44

F

false condition 6-1
 fan-in 6-17
 fan-out 6-17
 FET 4-1
 Field-Effect Transistor 4-1
 figure window in MATLAB A-13
 firing angle 4-26
 first harmonic 8-1
 first order all-pass filter. 5-96
 fixed bias 3-20
 fixed-bias circuit 7-21
 flash converter 5-55
 flash type ADC 5-55
 flat-staggered amplifier 29-1
 Flip Block in Simulink B-11
 flip-flop 7-21
fmin(f,x1,x2) MATLAB function A-25
 format MATLAB command A-29
 forward-biased diode 2-5
 Foster-Seely discriminator 2-36
 Foundation library in Simscape C-1
 Fourier series 8-1, 9-3
 four-layer diode 4-40
fplot MATLAB command A-25
 free electron 2-1
 free electron movement 2-2
 frequency response 1-5, A-11
 frequency spectrum 8-1, 9-3
 frequency-response curve 5-25

IN-2

full-wave rectifier 2-21, 2-23
 function file in MATLAB A-24
 fundamental frequency 8-1
zero MATLAB function A-25, A-27

G

Gain blocks in Simulink B-18
 gallium arsenide 3-2
 gate 4-1
 gate turn-off SCR 4-26
grid MATLAB command A-11
gtext('string') MATLAB command A-13
 GTO 4-26
 gyration resistance. 5-65

H

half power 5-9, 5-10
 half-power frequency 8-6, 9-9
 half-power points 1-5
 half-wave rectifier 2-18
 half-wave rectifier with limited
 negative output 5-48
 half-wave rectifier with limited
 positive output 5-47
 hard limiter. 2-32
 harmonics 9-3
 Hartley oscillator 10-7
 h-equivalent circuit 3-59
 hex buffer 6-36
 High level 6-1
 high-frequency models for
 transistors 3-54
 high-pass filter 1-22, 5-9
 High-Z output of tri-state devices 6-36
 hole 2-1
 hole movement 2-2
 h-parameter equivalent circuit 3-60
 hybrid incremental network
 model 3-48

I

IC (integrated circuit) 1-1
 ideal characteristics 2-6
 IGFET 4-6
 imag(z) MATLAB function A-22
 improper rational function 1-11
 impurity atoms 2-3
 incremental conductance 2-16
 incremental linear models 3-48
 incremental resistance 2-16
 increments between point
 in MATLAB A-13
 input clamp voltage 6-3, 6-13
 input resistance 5-21
 instrumentation amplifiers 5-41
 Insulated-Gate FET 4-6
 integrated circuit (IC) 1-1
 integrator 5-30

internal frequency compensation 5-44
 inverse active mode 6-5
 inverter 6-2
 inverting mode 5-2
 inverting summing circuit 5-37

J

JFET 4-1
 junction recombination 2-4

L

laser diodes 2-48
 LC Oscillators 10-5
 leading edge 7-16
 light-emitting diode 2-46
lims = MATLAB function A-25
 line driver 6-35
 linearity 5-61
linspace MATLAB command A-13
 ln (natural log) in MATLAB A-12
 load line 2-10, 3-39
 load line 3-39
 load resistance 5-23
 log in MATLAB A-12
log(x) MATLAB function A-12
log10(x) MATLAB function A-12
log2(x) MATLAB function A-12
loglog(x,y) MATLAB command A-12
 lossless coupling network 9-12
 low frequency amplifier 8-5
 Low level 6-1
 lower sidebands 9-4
 low-pass filter 1-5, 5-9

M

magnitude response 1-5
 majority carriers 2-3
 marginally stable 1-11
 Math Operations in Simulink B-11
 MATLAB Demos A-2
 MATLAB editor/debugger A-1
 matrix multiplication in MATLAB A-17
 maximum average forward current 2-7
 maximum surge current 2-8
 melted silicon 2-3
 MESFET 4-22
mesh(x,y,z) MATLAB command A-15
meshgrid(x,y) MATLAB command A-16
 Metal Oxide Semiconductor 4-1
 Metal Oxide-Semiconductor
 Field Effect Transistor 4-6
 Metal Semiconductor
 Field-Effect-Transistor 4-22
 m-file in MATLAB A-1, A-24
 microelectronics 1-1
 Miller effect 8-10
 Miller effect F-12
 Miller integrator 5-30

Miller's theorem F-10
 minority carriers 2-3
 modulation 9-1
 modulation index in AM systems 9-3
 monostable multivibrator 7-15
 MOSFET 4-1, 4-6
 mutual inductance 10-7

N

NaN in MATLAB A-25
 NAND gate 6-1
 narrowband approximations 9-14
 narrowband signals 9-3
 negative feedback 10-1
 negative logic 6-2
 negative resistance 2-44
 negative voltage limiter 5-45, 5-47
 NMOS Logic Gates 6-28
 non-inverting averaging 5-37
 non-inverting mode 5-5
 non-inverting op amp 5-13
 non-inverting summing 5-37
 norator 5-26
 NOT gate 6-1
 NPN transistor 3-1
 N-type semiconductor 2-3
 nullor 5-26
 Nyquist rate 5-61

O

octave defined 1-7
 offset null 5-43
 op amp 5-1
 open collector 6-18
 open-loop 5-24
 open-loop gain 5-26
 operational amplifier 5-1
 optical coupler 2-49
 optoelectronic devices 2-46
 optoisolator 2-49
 OR gate 6-1
 output conductance 4-12
 output resistance 5-23
 overcompensated attenuator E-2
 overstaggered amplifier 9-21

P

passive filter 5-8
 passive pull-up 6-18
 peak forward current 2-7
 peak point in UJT 4-23
 peak rectifier 2-30, 2-36, 9-2
 peak inverse voltage (PIV) 4-26
 peak reverse voltage 2-8
 peak-to-valley ratio 2-45, 9-21
 pentode region 4-9
 period 1-2
 periodic signals 8-1
 periodic time function 1-2
 phase response 1-5

phase shifter 5-96
 phase-modulated signal 9-1
 phase-shift oscillator 10-4
 photocell 2-48
 photodiode 2-48
 phototransistor 2-48
 physical network in Simscape C-1
 PID controller D-1
 piecewise-linear analysis 3-43
 Pierce oscillator 10-10
 pinch-off 4-3
 pinch-off voltage 4-8
plot(x,y) MATLAB command A-9, A-12
plot(x,y,'rs') MATLAB command A-14
plot(x,y,'rs-') MATLAB command A-14
plot(x,y,s) MATLAB command A-14
plot3(x,y,z) MATLAB command A-14
 PMOS device 6-30
 PNP transistor 3-1
 PNP diode 4-40
 polar plot in MATLAB A-23
polar(theta,r) MATLAB function A-22
 poles 1-11, 1-21, 8-28
poly(r) MATLAB function A-4
polyder(p) MATLAB function A-6, A-7
polyval(p,x) MATLAB function A-5
 positive and negative voltage limiter 5-45
 positive feedback 10-1
 positive logic 6-2
 positive voltage limiter 5-45, 5-47
powergui block in Simscape C-7
 programmable UJT 4-24
 proper rational function 1-11
 proportional-integral-derivative (PID) controller D-1
 PS-Simulink Converter block in Simscape C-3
 P-type semiconductor 2-3
 pulsating DC voltages. 2-25

Q

quadratic region 4-8
 quality factor 9-10
 quantization 5-60
 quantization error 5-61
 quartz crystal 10-8
 quiescent voltages and currents 3-18
quit MATLAB command A-2

R

R-2R ladder network, 5-52
 transconductance 1-18
 rational function 8-27
 rational polynomials A-7
 RC Oscillator 10-4
real(z) MATLAB function A-22
 recombination 2-2
 reduction theorem F-6
 regenerative feedback 10-2
 relaxation oscillators 10-1

resistive network 5-55
 resolution 5-61
 reverse-biased 2-5
 rise time E-1
 RMS value 1-2
 roots of polynomials in MATLAB A-3
roots(p) MATLAB function A-3, A-7
round(n) MATLAB function A-22
 row vector in MATLAB A-3, A-17
 rubidium oscillators 10-8

S

sampling 5-60
 sampling theorem 5-60
 saturation current 2-54
 Saturation Region 3-77
 saturation region 4-9
 Schmitt trigger 7-32
 Schottky diode 2-43, 6-39
 SCR 4-24
 script file in MATLAB A-24
 second harmonic 8-1
 self-bias 3-25
 self-bias flip-flop 7-24
 semicolon in MATLAB A-7
semilogx MATLAB command A-12
semilogy MATLAB command A-12
 series-fed tuned-collector 10-6
 Shockley diode 4-40
 silicon controlled rectifier 4-24
SimElectronics Library in Simscape C-4
SimPowerSystems library in Simscape C-7
 Simscape libraries C-1
 Simulink PID blocks D-2
 Simulink-PS Converter block in Simscape C-3
 single ended output 5-1
 single ended output amplifier 5-1
 single sideband 9-4
 single-slope converter 5-58, 5-59
 single-tuned transistor amplifier 9-8
 sinking current 6-18
 sinusoidal oscillators 10-1
 slew rate 5-44
 slope converter 5-55
 SN7400 Quad 2-input NAND gate 6-10
 SN7402 Quad 2-input NOR gate 6-14
 SN7404 Hex Inverter 6-3
 SN7407 Hex Buffer 6-36
 SN7408 Quad 2-input AND gate 6-6
 SN7417 hex buffer 6-36
 SN7432 Quad 2-input OR gate 6-8
 SN7486 Quad XOR gate 6-16
 SN74121 monostable multivibrator 7-16
 SN74125 quad bus buffer 6-36
 solar cell 2-48
Solver Configuration block in Simscape C-3
 source 4-1
 source absorption theorem F-4

- sourcing current 6-18
- stability 1-11, 5-16
- stable system 1-11
- stagger-tuned amplifiers 9-17
- string in MATLAB A-15
- subplot(m,n,p)** MATLAB
 - command A-16
- substitution theorem F-1
- successive approximation
 - type ADC 5-57
- summing circuit 5-16
- symmetrical triggering 7-30
- synchronously tuned amplifier 9-14

T

- T-equivalent circuit 3-59
- text(x,y,z,'string')** MATLAB
 - command A-15
- thermal voltage 2-6
- third harmonic 8-1
- threshold voltage 6-30
- thyristor 4-24
- tickler coil 10-5
- time-window converter 5-55
- title('string')** MATLAB command A-12
- totem-pole configuration 6-11
- tracking converter 5-55
- trailing edge 7-16
- transconductance 3-53, 4-2, 4-4, 4-11
- transistor 3-1
- transistor at high frequencies 8-9
- transistor networks 3-59
- Transistor-Transistor Logic (TTL) 6-2
- transition time 7-29
- transresistance 1-18
- transresistance amplifier 5-28
- transresistance gain 5-28
- triac 4-39
- triode region 4-8
- triple-point bandwidth 9-21
- triple-point frequencies 9-20
- tri-stated buffers 6-36
- true condition 6-1
- truth table for 2-input NMOS
 - NAND gate 6-31
- truth table for 2-input XNOR gate
 - with positive logic 6-17
- truth table for 2-input XOR gate 6-16
- truth table for 3-input NOR gate
 - with positive logic 6-14
- truth table for a 3-input AND gate 6-6
- truth table for a 3-input
 - NAND gate 6-9
- truth table for a 3-input OR gate 6-8
- tuned amplifier 9-1
- tunnel diode 2-44

U

- uncompensated attenuator 7-30
- uncompensated attenuator E-1
- undercompensated attenuator E-22
- understaggered amplifier 9-21
- unijunction transistor 4-23
- unipolar transistor 4-2
- unit load 6-17
- unit step function 5-32
- unity gain amplifier 5-8, 5-15
- unity gain frequency 5-24
- unstable 1-11
- unsymmetrical triggering 7-30
- upper sidebands 9-4

V

- varactor 2-46, 2-52
- varicap 2-46, 2-52
- VCC 5-1
- VCVS 5-12
- VEE 5-1
- virtual ground 5-12
- voltage amplifier 1-15
- Voltage Controlled Voltage
 - Source 5-12
- voltage doubler 2-35
- voltage follower 5-15
- voltage gain 4-18
- voltage quadruplers 2-35
- voltage source absorption F-4
- voltage triplers 2-35

W

- Wien bridge oscillator 5-49

X

- xlabel('string')** MATLAB
 - command A-12
- XNOR gate 6-1, 6-16
- XOR gate 6-1, 6-15

Y

- ylabel('string')** MATLAB
 - command A-12

Z

- Zener diode 2-37
- Zener region 2-7
- zeros 1-11, 1-21, 8-27